Semiconductor Electronics

SOLUTIONS

Exercise-I (Conceptual Questions)

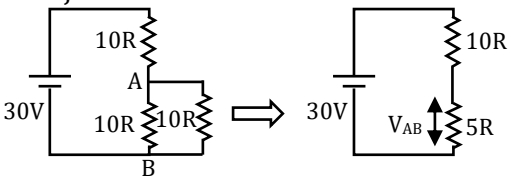
19. $n = AT^{3/2}e^{\frac{-\Delta Eg}{2kT}}$

35. When P-N junction is operated at 5mA

$(2 - 0.5) = 5 \times 10^{-3} \times R$

$R = 300\ \Omega$

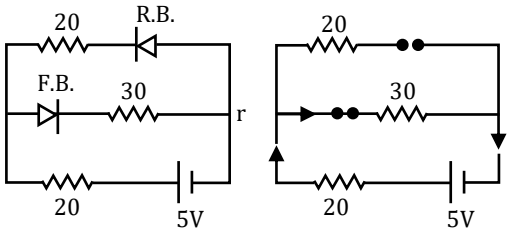
37. P-N junction in forward bias



$V_{AB} = IR' = \left(\frac{30}{15R}\right) \times 5R = 10V$

38. $I = \frac{3V - 1V}{100\Omega} = 20mA$

40.



$I = \frac{5}{50}A$

41. Electric field $= \frac{V}{d} = \frac{0.1}{10^{-6}} = 10^5$ (V/m)

49. To produce e–h pair

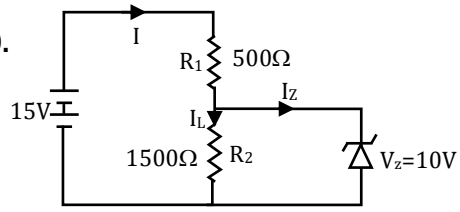
energy of incident photon $\geq \Delta E_g$

$\frac{hc}{\lambda} \geq \Delta E_g$

λ (In Å) $\leq \frac{12400}{\Delta E_g (\text{in eV})} \leq \frac{12400}{0.75} \leq 16500$ Å

So $\lambda_{max} = 16500$Å

50.



$10 = I_L R_L = I_L \times 1500$

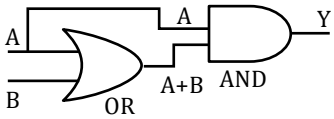
$I_L = 6.67$ mA

$I = \frac{V - V_z}{R_1} = \frac{15 - 10}{500} = \frac{5}{500} = 10mA$

$I = I_L + I_Z$

$I_Z = I - I_L = (10 - 6.67)mA = 3.33mA$

67.



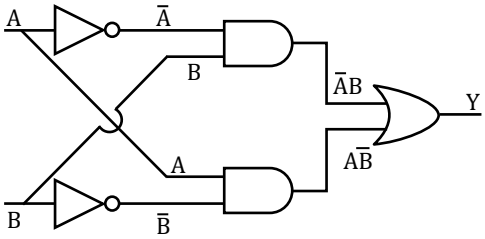
$Y = A.(A+B)$

$Y = A.A + AB$

$Y = A + AB = A(1+B)$

$Y = A$

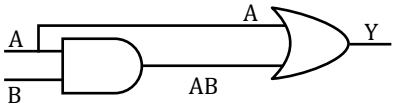
75.



$Y = \bar{A}B + A\bar{B}$

$= A \oplus B$ = XOR gate

76.



$Y = A + AB = A(1+B)$

$= A$

Exercise-II (Previous Year Questions)

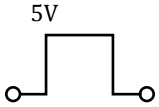
3. $y_1 = \bar{A}, y_2 = \bar{B}$,

$y = \overline{y_1 + y_2} = \overline{\bar{A} + \bar{B}}$ (using De-morgan's theorem)

$y = \bar{\bar{A}} \cdot \bar{\bar{B}} = A \cdot B$ AND gate

Hence this logic gate represents AND gate.

4. This is the circuit where P-N junction is acting as a Half-wave rectifier so the output will be



5. Potential difference on R = 3.5 – 0.5 = 3.0 volt

Current in circuit $i = \frac{V}{R} = \frac{3}{100} = 30mA$

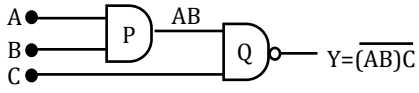
6. Since diode is in forward bias

$i = \frac{\Delta V}{R} = \frac{4 - (-6)}{1 \times 10^3} = \frac{10}{10^3} = 10^{-2}$ A

8. Current will not flow through D_1 as it is reverse biased. Current will flow through cell, R_1, D_2 and R_3.

$\therefore \quad i = \frac{10}{2+2} = 2.5\ A$

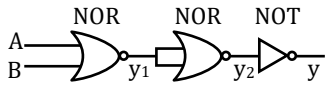
9.



for A = B = C = 0 ; y = 1

for A = B = C = 1 ; y = 0

10.

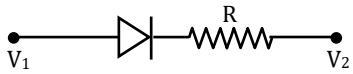


$y_1 = \overline{A + B}$

$y_2 = \overline{y_1 + y_1} = \overline{y_1} = \overline{\overline{A + B}} = A + B$

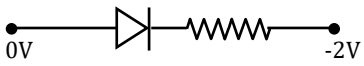
$y = \overline{y_2} = \overline{A + B}$ NOR GATE

11.



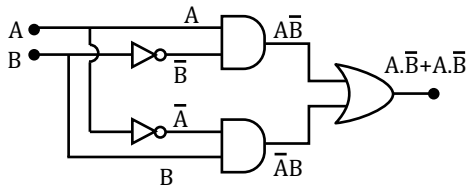
In forward bias $V_1 > V_2$

$\Rightarrow$ only



is in forward bias

12.



13. Due is heating, number of electron hold pairs will increase that affects the overall V – I characteristics of p-n junction

14.

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

$\therefore$ It is a NAND Gate

15. For P type

Holes are majority & trivalent atoms are the dopants.

16. $\lambda = \frac{1240\,nm}{1.9} = 652.6\ nm \simeq 654\ nm$

A	B	Y
0	0	1

17.

0	1	0	NOR gate
1	0	0	
1	1	0	

18. In reverse bias external battery attract majority charge carriers.

so width of the depletion region increase

19. In semiconductors and insulators, the number of charge carries per unit volume increases with an increase in temperature, so $\propto$ is negative for these.

20. $Y = \overline{\overline{A}+\overline{B}} = \overline{\overline{A}}.\overline{\overline{B}} = A.B$ = AND gate

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

21. In forward bias $V_P > V_N$

22. NAND gate and NOR gate are universal logic gates.

23. For N type semi-conductor intrinsic semiconductor doped by pentavalent impurity.

24. In N type semiconductor majority charge carriers are e and P type semiconductor majority charge carriers are holes.

$I = neAV_d = neA\ (\mu E)$

$\mu_e > \mu_h \quad \Rightarrow \quad I_e > I_h$

25. Reverse bias Zener diode is used a voltage regulator

for Ge Potential barrier $V_0 = 0.3$ V

Si Potential barrier $V_0 = 0.7$ V

26. $Y = A \cdot B + \overline{B \cdot C} = AB + \overline{B} + \overline{C}$

(i) 0 to t_1 A = 0, B = 0, C = 1

$Y = 0 \cdot 0 + \overline{0 \cdot 1} = 0 + 1 = 1$

(ii) t_1 to t_2 A = 1, B = 0, C = 1

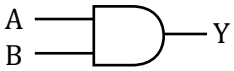
$Y = 1 \cdot 0 + \overline{0 \cdot 1} = 0 + 1 = 1$

(iii) t_2 to t_3 A = 0, B = 1, C = 0

$Y = 0 \cdot 1 + \overline{1 \cdot 0} = 0 + 1 = 1$

32. $Y = \overline{\bar{A}+\bar{B}} = \bar{\bar{A}}\cdot\bar{\bar{B}} = A.B$

AND gate

for AND gate 

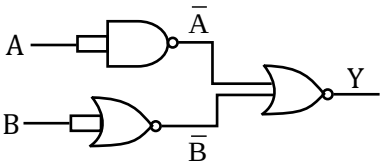
33. For p type semiconductor trivalent impurity added

34.

A	B	Y
0	0	1
0	1	0
1	0	1
1	1	0

According to truth table, relation is inverse between Y and B.

Here, $Y = \bar{B}$

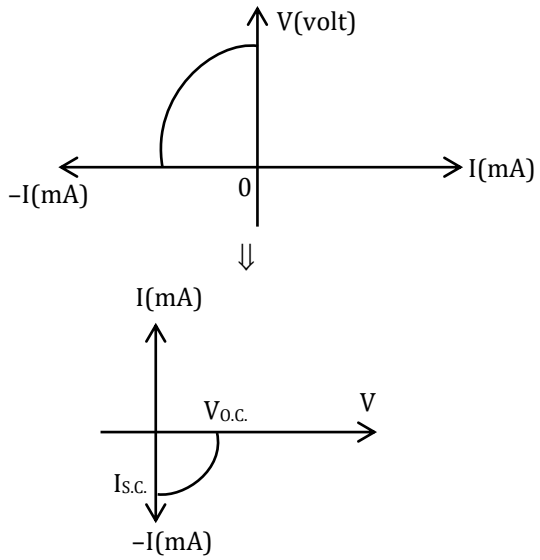
35. 

$\overline{\bar{A}+\bar{B}} \Rightarrow \bar{\bar{A}}\cdot\bar{\bar{B}} \Rightarrow A\cdot B$ (AND GATE)

36. A. Solar-cell, the I-V characteristics lie in the IV quadrant.

B. In reverse biased condition due to drift of minority charge carriers current flow in μA

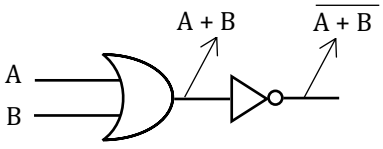
Answer should be (1) A is correct and (B) is incorrect

37. 

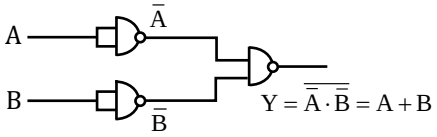
$V_{o.c.} \rightarrow$ Open circuit voltage

$I_{s.c.} \rightarrow$ short circuit voltage

Note : Graph of solar cell drawn in IV- Quadrant because it does not draw the current but supply same to the load.

38. 

$Y = \overline{A+B}$ (NOR gate)

39. 

Exercise-III (Analytical Questions)

1. Indium is a trivalent impurity.

4. When temp. increases in semiconductor then number of charge carriers increase.

6. In an unbiased P-N junction, majority charge carriers diffuse due to concentration difference.