CHAPTER 4

Semiconductor Devices and Applications

Learning Objectives

After reading this chapter, you will be able to understand concepts and problems based on:

(a) The basics of semiconductors
(b) Types of semiconductors
(c) Nature of charge carriers
(d) Junction diode basics
(e) Diode as a rectifier
(f) Zener Diode
(g) Opto electronic junction devices
(h) Transistor and its working
(i) Input and Output characteristics of a transistor
(j) Transistor as a switch
(k) Transistor as an Amplifier
(l) Transistor as an Oscillator
(m) Logic Gates and Applications.

All this is followed by an Exercise Set (fully solved) which contains questions as per the latest JEE pattern. At the end of Exercise Set, a collection of problems asked previously in JEE Main are also given.

INTRODUCTION

Devices in which a controlled flow of electrons can be obtained are the basic building blocks of all the electronic circuits.

Before the discovery of transistor in 1948, such devices were mostly vacuum tubes (also called valves) like

(a) a vacuum diode which has two electrodes i.e. an anode (often called plate) and a cathode.
(b) a triode which has three electrodes i.e. a cathode, a plate and a grid.
(c) a tetrode (with four electrodes) and
(d) a pentode (with five electrodes).

FUNCTIONING OF VACUUM TUBE(S)

In a vacuum tube, the electrons are supplied by a heated cathode and the controlled flow of these electrons in vacuum is obtained by varying the voltage between its different electrodes. Vacuum is required in the inter electrode space, else the moving electrons may lose their energy on collision with the air molecules in their path. In these devices the electrons can flow only from the cathode to the anode (i.e., only in one direction). *Therefore, such devices are generally referred to as valves.*

DISADVANTAGES OF USING VACUUM TUBE(S)

Vacuum tube devices are bulky, consume high power, operate generally at high voltages (~100 V) and have limited life and low reliability.

SEMICONDUCTOR ELECTRONICS

The seed of the development of modern solid-state semiconductor electronics goes back to 1930's when it was observed that some solid state semiconductors and their junctions offer the possibility of controlling the number and the direction of flow of charge carriers through them. Simple excitations like light, heat or small applied voltage can change the number of mobile charges in a semiconductor. Also note that the supply and flow of charge carriers in the

semiconductor devices are within the solid itself, whereas in the earlier vacuum tubes/valves, the mobile electrons were obtained from a heated cathode and they were made to flow through an evacuated space called vacuum. Semiconductor devices require no external heating or large evacuated space. They are small in size, consume low power, operate at low voltages and have long life and high reliability.

CLASSIFICATION OF METALS, CONDUCTORS AND SEMICONDUCTORS ON THE BASIS OF CONDUCTIVITY

On the basis of the relative values of electrical conductivity (σ) or resistivity $\left(\rho = \frac{1}{\sigma}\right)$, the solids are broadly classified as:

(a) Insulators: They have high resistivity or low conductivity.

$$\rho \approx 10^{11} - 10^{19}\ \Omega\text{m}$$

$$\sigma \approx 10^{-11} - 10^{-19}\ \text{Sm}^{-1}$$

(b) Metals: They have very low resistivity or high conductivity.

$$\rho \approx 10^{-2} - 10^{-8}\ \Omega\text{m}$$

$$\sigma \approx 10^{2} - 10^{8}\ \text{Sm}^{-1}$$

(c) Semiconductors: They have resistivity or conductivity whose values lie somewhere between metals and insulators.

$$\rho \approx 10^{-5} - 10^{6}\ \Omega\text{m}$$

$$\sigma \approx 10^{5} - 10^{-6}\ \text{Sm}^{-1}$$

The values of ρ and σ given above are indicative of magnitude and could well go outside the ranges as well.

Relative values of the resistivity are not the only criteria for distinguishing metals, insulators and semiconductors from each other. Our interest in this chapter is in the study of semiconductors which could be:

(a) Elemental semiconductors like *Si* and *Ge*
(b) Compound semiconductors like
- **Inorganic:** *CdS*, *GaAs*, *CdSe*, *InP*, etc.
- **Organic:** anthracene, doped pthalocyanines, etc.
- **Organic polymers:** polypyrrole, polyaniline, polythiophene, etc.

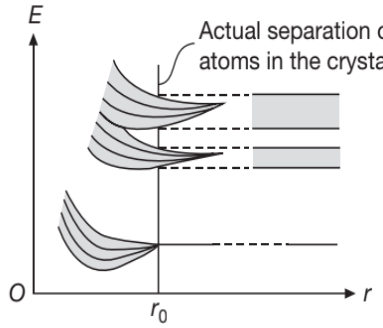
Conceptual Note(s)

Most of the currently available semiconductor devices are based on elemental semiconductors Si or Ge and compound inorganic semiconductors. However, after 1990, a few semiconductor devices using organic semiconductors and semiconducting polymers have been developed signalling the birth of a futuristic technology of polymer- electronics and molecular-electronics.

However, in this chapter, we shall be restricting ourselves to the study of inorganic semiconductors, particularly elemental semiconductors Si and Ge. The general concepts introduced here for discussing the elemental semiconductors, by-and-large, apply to most of the compound semiconductors as well.

ENERGY BANDS

For an isolated atom, the valence electrons can exist only in one of the allowed orbitals each of a sharply defined energy called energy levels. However, when two atoms are brought nearer to each other, then there are alterations in energy levels and they spread in the form of bands as shown in Figure.



Origin of energy bands in a solid

Valence Band

The energy band formed by a series of energy levels containing valence electrons is known as **valence band**. At 0 K, the electrons fill the energy levels in valence band starting from lowest one. It must be noted that

(a) this band is always filled with electrons.
(b) this is the band of maximum energy till which an electron stays in the valence shell of an atom.
(c) there is no flow of current due to electrons present in this band.

Fermi Level

The highest energy level which can be occupied by an electron in valence band at 0 K is called **Fermi Level**.

Conduction Band

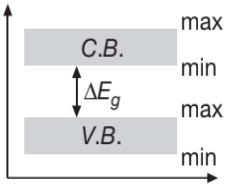
The lowest unfilled allowed energy band next to valence band is called **conduction band**. At 0 K the Fermi Level and other lower levels are occupied completely by electrons. As temperature rises, the electrons absorb energy and get excited and jump to higher levels. The electrons in higher energy levels are more free as compared to electrons in the lower energy levels. It must be noted that

(a) this band is also called an empty band of minimum energy because, after that if the energy increases, then the electrons become free and are not bound to the nucleus
(b) this band is partially filled by the electrons.
(c) The electrons in the conduction band are called the free electrons. They are able to move anywhere within the volume of the solid.
(d) Current flows due to such electrons.

FORBIDDEN ENERGY GAP (ΔE_g)

The energy gap between the conduction band and the valence band is called the Forbidden Energy Gap, given by

$$\Delta E_g = (C.B.)_{min} - (V.B.)_{max}$$



It must be noted that

(a) no free electron is present in forbidden energy gap.
(b) width of forbidden energy gap depends upon the nature of substance.
(c) as temperature increases, the forbidden energy gap decreases very slightly.

For Conductors, $\Delta E_g < 0.1$ eV

For Insulators, $\Delta E_g > 3$ eV

For Semi-conductors, $0.1 \text{ eV} < \Delta E_g < 3$ eV

For Germanium, $\Delta E_g = 0.7$ eV

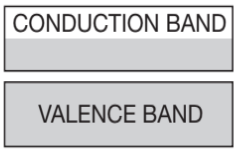
For Silicon, $\Delta E_g = 1.1$ eV

BAND THEORY OF CLASSIFICATION OF METALS, INSULATORS AND SEMICONDUCTORS

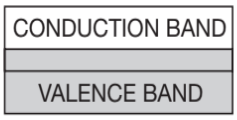
Metals

In this case we have two possibilities

(a) The valence band completely filled and conduction band partially filled and extremely small energy gap between valence band and conduction band. e.g. In sodium, conduction band is partially filled while valence band is completely filled.



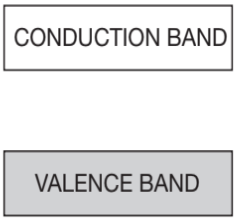
(b) The valence band is completely filled and conduction band is empty and two overlap each other. e.g. Zinc.



In both the cases it can be assumed that there is a single energy band which is partially filled and hence on application of small electric fields metals conduct electricity.

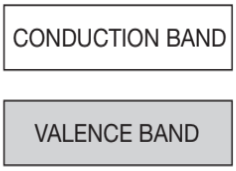
Insulators

In insulators the Forbidden Energy Gap (FEG) is quite large e.g. In case of diamond FEG is of order of 6 eV i.e. a minimum of 6 eV of energy is required by an electron to jump from completely filled valence band to conduction band. When electric field is applied across such a solid the electrons find it difficult to acquire this large amount of energy and so conduction band continues to be almost empty.



Semiconductors

The energy band structure is similar to that of insulators but in the case of semiconductors the Forbidden Energy Gap (FEG) is much smaller e.g. in case of silicon it is (FEG) 1.1 eV and because of smaller width of FEG the electrons in valence band find it comparatively easier to shift to conduction band even at room temperature.

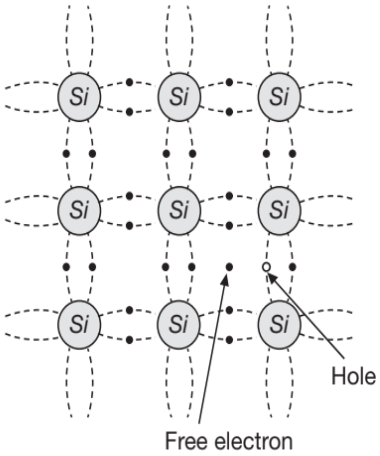


HOLES IN SEMICONDUCTORS

When an electron is removed from a covalent bond, it leaves a vacancy behind. An electron from a neighbouring atom can move into this vacancy, leaving the neighbour with a vacancy. In this way the vacancy formed is called hole (or cotter), and can travel through the material and serve as an additional current carriers. A hole is considered as a seat of positive charge, having magnitude of charge equal to that of an electron. A hole acts as a virtual charge, although it does not carry any physical charge on it. The effective mass of hole is more than electron, because the mobility of a hole is less than that of an electron.

CURRENT CARRIERS IN SEMICONDUCTORS

In a pure semiconductor, an atom behaves as if there are 8 electrons in its valence shell (because of formation of covalent bonds) and the entire material behaves as an insulator at low temperature. A semiconductor atom needs energy of order of 1.1. eV which is easily available at room temperature. Due to thermal agitation of crystal structure, electrons from a few covalent bonds come out and the bond from which an electron comes out has a vacancy called **Hole** (of positive nature).



This hole can be filled by some other electron from some other covalent bond. As the electron from some other covalent bond moves to fill this vacancy a hole is created at its place. In other words we can say that hole has shifted its position from one covalent bond to another as an electron does this in an attempt to fill the hole.

Conceptual Note(s)

Since a hole moves in a direction opposite to that of an electron so a hole is treated as a positive charged carrier.

So, at room temperature a pure semiconductor will have electrons and holes wandering in random directions. These electrons and holes are called **Intrinsic Carriers** and such a semiconductor is called an **Intrinsic Type Semiconductor**.

As a crystal is electrically neutral, the number density of free electrons n_e will be equal to number density of holes n_h. So, in an intrinsic semiconductor, $n_e = n_h = n_i$.

The fraction of electrons of valence band present in conduction band at temperature T is

$$f \propto \exp\left(\frac{-E_g}{k_B T}\right).$$

where E_g is the forbidden energy gap and k_B is Boltzmann constant.

INCREASING THE CONDUCTIVITY OF A SEMICONDUCTOR: DOPING PROCESS

A pure semiconductor at room temperature possesses free electrons and holes but their number is so small that conductivity offered by the pure semiconductor cannot be of any practical use. By the addition of impurities to the pure semiconductor in a very small ratio $(1:10^6)$, the conductivity of a *Si*-crystal (or *Ge*-crystal) can be remarkably improved.

The process of adding impurity to a pure semi conductor crystal (*Si* or *Ge*-crystal) so as to improve its conductivity, is called **doping**.

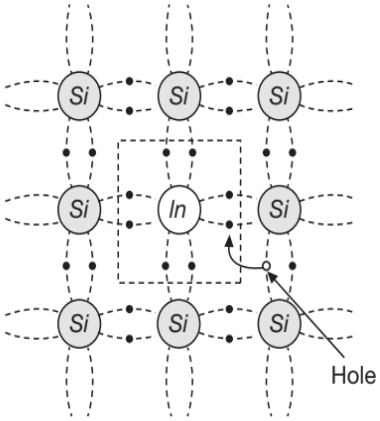
Generally, doping of few ppm i.e. 1 impurity atom per 10^6 semiconductor atoms is done. Also, the size of the dopant and the semiconductor atoms must be comparable or nearly same so that the dopant does not distort the original semiconductor lattice.
The impurity atoms are of two types:

(a) **Pentavalent impurity atoms** i.e. atoms having 5 valence electrons such as Antimony (*Sb*) or Arsenic (*As*). Such atoms, when added to a pure semiconductor, produce excess of free electrons i.e. donate electrons to the semiconductor. For this reason, pentavalent impurity atoms are called **Donor Impurity** atoms. The semiconductor so produced is called *n*-type **Extrinsic Semiconductor.**

(b) **Trivalent impurity atoms** i.e. atoms having 3 valence electrons such as Indium (*In*) or Gallium (*Ga*). Such atoms on being added to a pure semiconductor, instead of producing free electrons, accept electrons from the semiconductor. For this reason, trivalent impurity atoms are called **Acceptor Impurity** atoms. The semiconductor so produced is called *p*-type **Extrinsic Semiconductor.**

p-TYPE (EXTRINSIC) SEMICONDUCTOR

Consider a Silicon crystal to which a trivalent impurity say Indium is added. The four silicon atoms surrounding the *In* atom, can share one electron each with the *In* atom which has got three valence electrons. In an attempt to have 8 electrons in valence shell, the *In* atom borrows one of the nearby covalent bonds of one electron. Thus, the valence shell of the *In* atom possesses 8 electrons but a hole is created in the covalent bond from which electron has been borrowed.

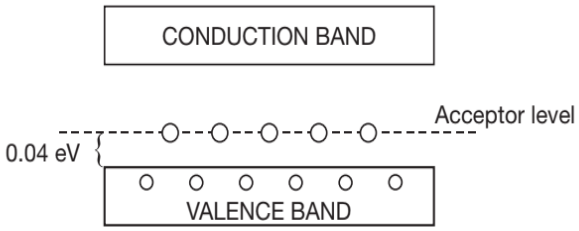


So, for every trivalent impurity atom added, an extra hole will be created. As the trivalent impurity atoms accept electrons from the silicon crystal, it is called **acceptor impurity**.

The *Si*-crystal so obtained is called *p*-type as it contains excess free holes. Each hole is equivalent to positive charge. The holes so created are extrinsic carriers and the *p*-type *Si*-crystal obtained is called *p*-type extrinsic semiconductor.

Since the pure *Si*-crystal also possesses a few electrons and holes (by way of thermal agitation), therefore, the *p*-type *Si*-crystal will have a large number of holes (majority charge carriers) and a small number of electrons (minority charge carriers).

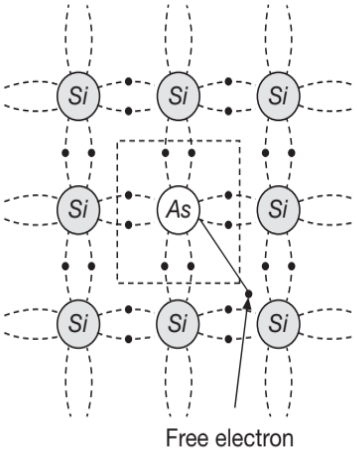
In the extrinsic *p*-type *Si*-crystal, the hole produced revolves round the nucleus of the *In* atom. Since the hole may be treated as a particle of same mass as electron but having an equal positive charge so, it possesses a small positive energy of the order of 0.04 eV. Such holes create an **acceptor energy level** (of value 0.04 eV) just above the top of the valence band. The electrons from valence band can raise themselves to the acceptor energy level by absorbing thermal energy at room temperature and in turn create holes in the valence band.



Number density of valence band holes (n_h) in p-type semiconductor is approximately equal to that of the acceptor atoms (N_a) and is very large as compared to the number density of conduction band electrons (N_e). Hence, $n_h \approx N_a >> n_e$.

n-TYPE (EXTRINSIC) SEMICONDUCTOR

When the arsenic impurity atoms are added to the silicon crystal in a small ratio $(1:10^6)$, its atoms replace the silicon atoms here and there. The four electrons out of the five valence electrons of *As* atom take part in covalent bonding with four silicon atoms surrounding it. The fifth electron is set free. Obviously, the extra free electrons created in the crystal will be as many as the number of the pentavalent impurity atoms added.



Since the pentavalent impurity increases the number of free electrons, it is called **donor impurity**. The silicon crystal so obtained is termed as n-type *Si* crystal. The electrons so set free in the silicon crystal are called **Extrinsic Carriers** and the n-type *Si* crystal is called n-type **Extrinsic Semiconductor**.

Due to thermal agitation, the pure *Si* crystal possesses a new electrons and holes. So, n-type *Si* crystal will have a large number of free electrons (majority charge carriers) and a small number of holes (minority charge carriers).

In the extrinsic n-type semiconductor, the fifth electron of the *As* atom revolves around the donor atom inside the *Si* crystal. As dielectric constant of silicon is very high, it is bound to the donor atom with a very small amount of energy, which is of the order of 0.045 eV. In terms of valence and conduction band, one can think that all such electrons (extrinsic carriers) create a donor energy level just below (0.045 eV) the conduction band as shown in figure. As the energy gap between donor energy level and the conduction band is very small, the electrons can easily raise themselves to conduction band even at room temperature. Hence, the conductivity of n-type extrinsic semiconductor is remarkably increased.

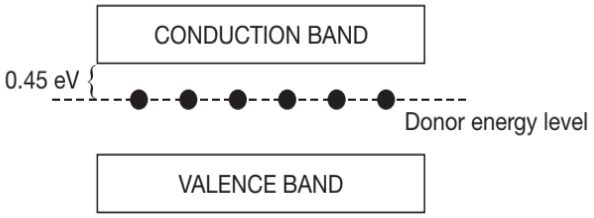


ILLUSTRATION 1

A p-type semiconductor has acceptor level 50 meV above the valence band. Find the maximum wavelength of light that can create a hole.

SOLUTION

To create a hole, an electron of valence band has to be excited into one of the acceptor levels which are 50 meV above the valence band. Hence a minimum of 50 meV energy is needed to create a hole. Since

$$E_{\min} = \frac{hc}{\lambda_{\max}}$$

$$\Rightarrow \quad \lambda_{\max} = \frac{hc}{E_{\min}} = \frac{6.6\times10^{-34}\times3\times10^{8}}{50\times1.6\times10^{-22}}$$

$$\Rightarrow \quad \lambda_{\max} = 2.47\times10^{-5}\ \text{m}$$

RELATION BETWEEN THE NUMBER DENSITY OF INTRINSIC AND EXTRINSIC CHARGE CARRIERS

In a doped or extrinsic semiconductor, the number density of the conduction band (n_e) and the number density of holes in the valence band (n_h) differ from that in a pure semiconductor. If n_i is the number density of electrons in conduction band or the number density of holes in valence band in a pure semiconductor, then

$$n_e n_h = n_i^2$$

This relation is also called as Mass-Action Law.

In n-type (extrinsic) semiconductor, the number density of electrons in conduction band is approximately equal to that of donor atoms and very large as compared to number density of holes in valence band. Thus,

$$n_e \approx N_d >> n_h,$$

where N_d represents the number density of donor atoms.

ILLUSTRATION 2

A semiconductor has equal electron atom hole concentration of $6\times10^{8}\ \text{m}^{-3}$. On doping with certain impurity, electron concentration increases to $9\times10^{12}\ \text{m}^{-3}$.

(i) Identify the new semiconductor obtained after doping.
(ii) Calculate the new hole concentration.
(iii) How does the energy gap vary with doping?

SOLUTION

(i) Since the electron concentration increases after doping, so the new semiconductor is an n type semiconductor.

(ii) Since, $n_e n_h = n_i^2$

where, $n_i = 6\times10^{8}\ \text{m}^{-3}$, $n_e = 9\times10^{12}\ \text{m}^{-3}$

$$\Rightarrow \quad n_h = \frac{n_i^2}{n_e} = \frac{(6\times10^{8})^2}{9\times10^{12}}$$

$$\Rightarrow \quad n_h = 4\times10^{4}\ \text{m}^{-3}$$

(iii) Doping decreases the energy gap.

ILLUSTRATION 3

A germanium specimen is doped with aluminium. The concentration of acceptor atoms is nearly $10^{21}\ \text{m}^{-3}$. Given that the intrinsic concentration of electron hole pairs is about $10^{19}\ \text{m}^{-3}$, then calculate the concentration of electrons in the specimen.

SOLUTION

According to Mass-Action Law, we have

$$n_i^2 = n_h n_e$$

where, $n_i \approx 10^{19}\ \text{m}^{-3}$ is the number density of intrinsic charge carriers and $n_h \approx 10^{21}\ \text{m}^{-3}$ is the number density of acceptor atoms.

$$\Rightarrow \quad n_e = \frac{n_i^2}{n_h} = \frac{(10^{19})^2}{(10^{21})} = 10^{17}\ \text{m}^{-3}$$

ILLUSTRATION 4

In a pure germanium sample taken at a temperature of $300\ \text{K}$, concentration of electron-hole pairs is $7\times10^{15}\ \text{cm}^{-3}$. If one antimony atom is doped into germanium for 10^{7} germanium atoms and assuming that only half of the impurity atoms contribute electrons to the conduction band, then calculate the factor by which the number of charge carriers increase due to doping. Assume that the number density of the germanium atoms is $5\times10^{28}\ \text{m}^{-3}$.

SOLUTION

The electron-hole pair concentration in a pure semiconductor is given to be $7\times10^{15}\ \text{m}^{-3}$. Total number density of charge carriers will be

$$n_{\text{initial}} = n_h + n_e = 14\times10^{15}\ \text{m}^{-3}$$

After doping is done with the donor impurity, we have

$$N_D = \frac{5\times10^{28}}{10^{7}} = 5\times10^{21}\ \text{m}^{-3}$$

and $n_e = \dfrac{N_D}{2} = 2.5\times10^{21}\ \text{m}^{-3}$

So, $n_{\text{final}} = n_h + n_e$

Since, we have $n_e \gg n_h$, so

$$n_{\text{final}} \approx n_e \approx 2.5\times10^{21}\ \text{m}^{-3}$$

The factor (f) by which the number of charge carriers increase due to doping is given by

$$f = \frac{n_{\text{final}} - n_{\text{initial}}}{n_{\text{initial}}}$$

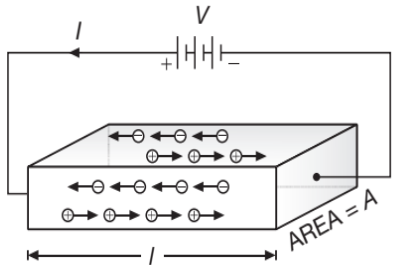
$$\Rightarrow \quad f = \frac{2.5\times10^{21} - 14\times10^{15}}{14\times10^{15}}$$

$$\Rightarrow \quad f \approx \frac{2.5\times10^{21}}{14\times10^{15}} = 1.8\times10^{5}$$

ELECTRICAL RESISTIVITY OF SEMICONDUCTORS

Consider a block of semiconductor of length l area of cross section A having n_e as number density of electrons and n_h as number density of holes. Then total current

$$I = I_e + I_h$$



Further $I_e = neAv_e$ and $I_h = n_h eAv_h$, where

v_e = Drift velocity of electrons and v_h = drift velocity of holes.

$$\Rightarrow \quad I = n_e eAv_e + n_h eAv_h$$

$$\Rightarrow \quad \frac{V}{R} = eA\left(n_e v_e + n_h v_h\right)$$

Since $V = El$ and $R = \frac{\rho l}{A}$

$$\Rightarrow \quad \frac{El}{\frac{\rho l}{A}} = eA\left(n_e v_e + n_h v_h\right)$$

$$\Rightarrow \quad \frac{1}{\rho} = \sigma = e\left\{n_e\left(\frac{v_e}{E}\right) + n_h\left(\frac{v_h}{E}\right)\right\}$$

$$\Rightarrow \quad \sigma = e\left(n_e\mu_e + n_h\mu_h\right)$$

where $\mu_e = \frac{v_e}{E}$ = Drift velocity of electrons per unit electric field also called **Electron Mobility**.

And $\mu_h = \frac{v_h}{E}$ = Drift velocity of holes per unit electric field also called **Hole Mobility**.

Conceptual Note(s)

Following points may be noted about the behaviour of semiconductors.

(a) At low temperature, a pure semiconductor behaves as an insulator. It becomes slightly conducting at room temperature due to thermal agitation process as a result of which a few electrons in the valence band acquire energy greater than the forbidden energy gap and move to the conduction band.

(b) It is very difficult to obtain an extremely pure semiconductor. In practice, an intrinsic semiconductor is that in which the concentration of impurity atoms is less than the concentration of intrinsic carriers.

(c) Extremely small doping can drastically change the conductivity of an intrinsic semiconductor.

(d) Electron mobility is greater than the hole mobility in semiconductors.

(e) At low temperature the semiconductors are insulators but become slightly conducting at room temperature. Thus, unlike metals, the resistance of semiconductors decreases with increase of temperature. Hence, they (semiconductors) possess a negative temperature coefficient of resistance (TCR).

(f) If light of energy greater than forbidden energy gap is incident on an intrinsic semiconductor, the electrons from the valence band move to the conduction band. Thus, electron and hole pairs are created. Due to increase in concentration of carriers, the conductivity of semiconductor increases. This property of semiconductors is called **photoconductivity.** Semiconductors with large photoconductivity are used as **Light Dependent Resistors (LDR)** which are commonly used in automatic light control circuits.

ILLUSTRATION 5

An n-type semiconductor of conductivity $6\ \Omega^{-1}\text{cm}^{-1}$ is to be made from an intrinsic germanium semiconductor. Calculate the number density of donor atoms required, if the mobility of electrons in n-type semiconductor is given to be $3850\ \text{cm}^2\text{V}^{-1}\text{s}^{-1}$.

SOLUTION

In n-type semiconductor, $n_e \gg n_h$

Let number density of donor atoms, $N_0 = n_e$

Conductivity of semiconductor is given by

$$\sigma = n_e e\mu_e$$

On substituting the values, we get

$$6\times10^2 = n_e \times 1.6\times10^{-19}\times3850\times10^{-4}$$

$$\Rightarrow \quad n_e = 9.7\times10^{21}\ \text{m}^{-3}$$

ILLUSTRATION 6

Calculate the conductivity of pure silicon crystal at 300 K temperature, if the electron hole pairs per cm^3 are 1.072×10^{10} at this temperature and mobilities are $\mu_h = 1350\ \text{cm}^2\text{V}^{-1}\text{s}^{-1}$ and $\mu_e = 480\ \text{cm}^2\text{V}^{-1}\text{s}^{-1}$.

SOLUTION

Conductivity of intrinsic i.e. pure silicon semiconductor is given by

$$\sigma = n_i e\mu_e + n_i e\mu_h = n_i e(\mu_e + \mu_h)$$

where n_i is the number density of intrinsic charge carriers, μ_e and μ_h are the mobility of electron and holes respectively.

Given that, $n_i = 1.072\times10^{10}\ \text{cm}^{-3}$

$\mu_h = 1350\ \text{cm}^2\ \text{volt}^{-1}\text{s}^{-1}$

$\mu_c = 480\ \text{cm}^2\ \text{volt}^{-1}\text{s}^{-1}$

$\Rightarrow \quad \sigma = (1.072\times10^{10})(1.6\times10^{-19})(1350+480)$

$\Rightarrow \quad \sigma = 3.14\times10^{-6}\ \Omega^{-1}\text{cm}^{-1}$

ILLUSTRATION 7

The energy gap of pure silicon semiconductor is 1.12 eV. The mobilities of electrons and holes are respectively $0.140\ \text{m}^2\text{V}^{-1}\text{s}^{-1}$ and $0.050\ \text{m}^2\text{V}^{-1}\text{s}^{-1}$. They are independent of temperature. The intrinsic carrier concentration is given by $n_i = n_0 e^{-\frac{E_g}{2k_BT}}$ where n_0 is a constant, E_g the gap width and k_B is the Boltzmann's constant whose value is $1.38\times10^{-23}\ \text{JK}^{-1}$. Calculate the ratio of the electrical conductivities of silicon at temperatures of 400 K and 200 K.

SOLUTION

Conductivity of semiconductor is given by

$$\sigma = n_e e\mu_e + n_h e\mu_h$$

where, $n_e = n_h = n_i$ (for a pure semiconductor)

$$\Rightarrow \quad \sigma = n_i e(\mu_e + \mu_h) = e(\mu_e + \mu_h)n_i$$

$$\Rightarrow \quad \sigma = e(\mu_e + \mu_h)n_0 e^{-\frac{E_g}{2k_BT}}$$

$$\Rightarrow \quad \frac{\sigma_{400}}{\sigma_{200}} = \frac{e^{\frac{-E_g}{2k_B(400)}}}{e^{\frac{-E_g}{2k_B(200)}}} = e^{\frac{E_g}{800k_B}}$$

$$\Rightarrow \quad \frac{\sigma_{400}}{\sigma_{200}} = e^{\frac{1.12\times1.6\times10^{-19}}{800\times1.38\times10^{23}}} = e^{16.23}$$

ILLUSTRATION 8

Calculate the resistivity of a sample in which 10^{19} atoms of phosphorous are added per cubic metre. Take the resistivity of pure silicon as 3000 ohm-metre and the mobilities of electrons and holes as $0.15\ \text{m}^2\text{V}^{-1}\text{s}^{-1}$ and $0.030\ \text{m}^2\text{V}^{-1}\text{s}^{-1}$ respectively.

SOLUTION

The conductivity of a pure silicon is given by

$$\sigma_i = n_i e(\mu_e + \mu_h)$$

Since the resistivity is reciprocal of conductivity, so

$$\rho_i = \frac{1}{\sigma_i} = \frac{1}{n_i e(\mu_e + \mu_h)}$$

$$\Rightarrow \quad n_i = \frac{1}{\rho_i e(\mu_e + \mu_h)}$$

$$\Rightarrow \quad n_i = \frac{1}{3000\times1.6\times10^{-19}(0.15+0.030)}$$

$$\Rightarrow \quad n_i = 1.157\times10^{16}\ \text{m}^{-3}$$

When 10^{19} atoms of phosphorus (donor atoms) are added per m^3, we have

$$n_e \gg n_i \text{ or } n_e \gg n_h$$

$$\Rightarrow \quad n_e = 10^{19}$$

$$\Rightarrow \quad \rho = \frac{1}{n_e e\mu_e} = \frac{1}{10^{19}\times1.6\times10^{-19}\times0.15}$$

$$\Rightarrow \quad \rho = 4.17\ \text{ohm metre}$$

p-n JUNCTION

A *p-n* junction is the basic building block of many semiconductor devices like diodes, transistor, etc. A clear understanding of the junction behaviour is important to analyse the working of other semiconductor devices. Let us now understand how a junction is formed and how the junction behaves under the influence of external applied voltage (also called bias).

p-n Junction Formation

Consider a thin *p*-type silicon $(p\text{-}Si)$ semiconductor wafer. By the precise addition of a small quantity of pentavalent impurity to this *p*-type silicon $(p\text{-}Si)$

semiconductor, a part of the p-Si wafer can be converted into n-type silicon $(\text{n-}Si)$. The wafer now contains p-region and n-region and a metallurgical junction between p and n-region.

Conceptual Note(s)

A p-n junction cannot be made just by placing a p-type semiconductor in close contact with n-type semiconductor. The two separate semiconductors cannot have a continuous contact at the atomic level. The junction will behave as a discontinuity for the flowing charge carries. So, both acceptor and donor impurities must be grown in a single Si or Ge crystal.

Diffusion Current, Drift Current and Barrier Potential

It is observed that two important processes occur during the formation of a p-n junction

1. Diffusion Process
2. Drift Process

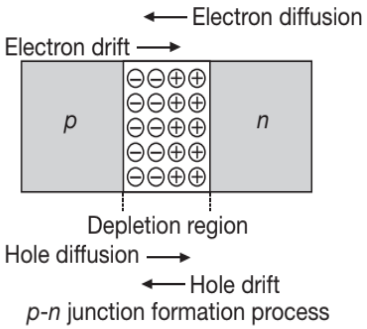
Since we know that in an n-type semiconductor, the concentration of electrons (number of electrons per unit volume) is more compared to the concentration of holes. Similarly, in a p-type semiconductor, the concentration of holes is more than the concentration of electrons. So, when the pn junction is formed, then due to the concentration gradient across p and n-sides, the holes diffuse from p-side to n-side $(p \to n)$ and electrons diffuse from n-side to p-side $(n \to p)$. *This motion of charge carriers due to diffusion from one region to the other gives rise to diffusion current* i_{df} *across the junction.*

Now, when an electron diffuses from $n \to p$, it leaves behind an ionised donor on n-side. This ionised donor (positive charge) is immobile as it is bonded to the surrounding atoms. As the electrons continue to diffuse from $n \to p$, a layer of positive charge (or positive space-charge region) on n-side of the junction is developed.

Similarly, when a hole diffuses from $p \to n$ due to the concentration gradient, it leaves behind an ionised acceptor (negative charge) which is immobile. As the holes continue to diffuse, a layer of negative charge (or negative space-charge region) on the p-side of the junction is developed.

This space-charge region on either side of the junction together is known as depletion region as the electrons and holes taking part in the initial movement across the junction depleted the region of its free charges (shown in figure). The thickness of depletion region is of the order of one-tenth of a micrometre.

Due to the positive space-charge region on n-side of the junction and negative space charge region on p-side of the junction, an electric field directed from positive charge towards negative charge develops. Because of this field, an electron on p-side of the junction moves to n-side and a hole on n-side of the junction moves to p-side. *This motion of charge carriers due to the electric field is called drift. Hence, a drift current* i_{dr}, *which is opposite in direction to the diffusion current (shown in figure) starts.*



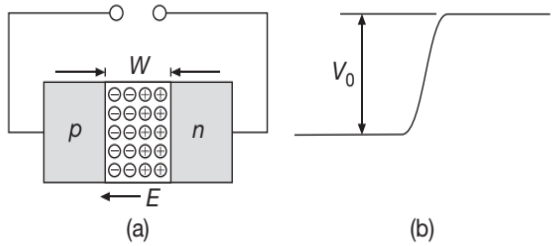
p-n junction formation process

Initially, diffusion current is large and drift current is small. As the diffusion process continues, the space-charge regions on either side of the junction extend, thus increasing the electric field strength and hence the drift current.

This process continues until the diffusion current equals the drift current. Thus, a p-n junction is formed. So, in this case

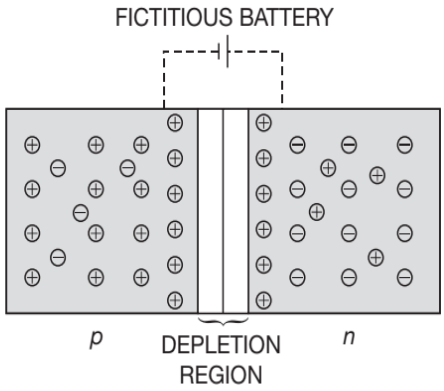
$$i_{\text{net}} = i_{df} + i_{dr} = 0$$

Since, in a p-n junction, under equilibrium there is no net current, so the loss of electrons from the n-region and the gain of electron by the p-region causes a difference of potential across the junction of the two regions. The polarity of this potential is such as to oppose further flow of carriers so that a condition of equilibrium exists. Figure shows the p-n junction at equilibrium and the potential across the junction.



(a) Diode under equilibrium ($V = 0$)
(b) Barrier potential under no bias.

The n-material has lost electrons, and p-material has acquired electrons. The n-material is thus positive relative to the p-material. Since this potential tends to prevent the movement of electron from the n-region into the p-region, it is often called a barrier potential. As a result of this it appears to us as if some fictitious battery is applied across the junction with its negative terminal connected to p region and positive terminal to n region.



The potential difference developed across the junction due to migration of majority charge carriers is called **potential barrier**. The potential barrier is of 0.7 V for Silicon and 0.3 V for Germanium.

On the average the potential barrier in pn junction is of the order of 0.5 V and the width of depletion region is of the order of 10^{-6} m, so the barrier electric field is

$$E = \frac{V}{d} = \frac{0.5}{10^{-6}} = 5\times10^{5}\ \text{Vm}^{-1}$$

ILLUSTRATION 9

A potential barrier of 0.5 V exists across a p-n junction.

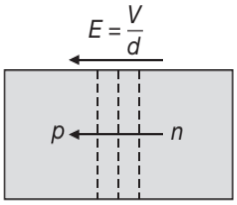
(i) If the depletion region is 5×10^{-7} m wide. Calculate the intensity of the electric field in the region.

(ii) If an electron having a speed of 5×10^{5} ms^{-1} approaches the junction from the n-side, calculate the speed with which it enters the p-side.

SOLUTION

(i) Width of depletion layer, $d = 5\times10^{-7}$ m

Electric field, $E_B = \frac{V}{d} = \frac{0.5\ \text{V}}{5\times10^{-7}} = 10^{6}$ volt m^{-1}



(ii) According to the Work-Energy Theorem, we have

$$W = \Delta K$$

$$\Rightarrow \quad eV = \frac{1}{2}m_e v_f^2 - \frac{1}{2}m_e v_i^2$$

$$\Rightarrow \quad \frac{1}{2}m_e v_i^2 = eV + \frac{1}{2}m_e v_f^2$$

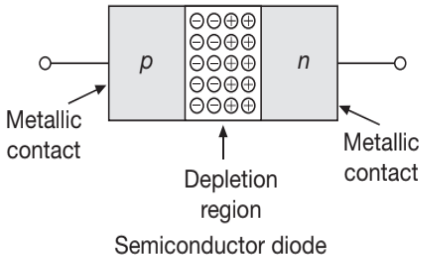
$$\Rightarrow \quad v_f = \sqrt{\frac{m_e v_i^2 - 2\ \text{eV}}{m_e}}$$

$$\Rightarrow \quad v_f = \sqrt{\frac{9\times10^{-31}\times(5\times10^{5})^2 - 2\times1.6\times10^{-19}}{9\times10^{-31}}}$$

$$\Rightarrow \quad v_f = 2.7\times10^{5}\ \text{ms}^{-1}$$

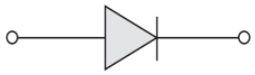
SEMICONDUCTOR DIODE

A semiconductor diode is basically a p-n junction with metallic contacts provided at the ends for the application of an external voltage as shown in Figure.



Semiconductor diode

It is a two terminal device. A p-n junction diode is symbolically represented as shown in Figure.



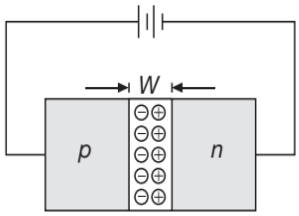
Symbol for *p-n* junction diode.

The direction of arrow indicates the conventional direction of current (when the diode is under forward bias). The equilibrium barrier potential can be altered by applying an external voltage V across the diode. In both the cases the diode is not connected across a voltage i.e. the diode is not biased and hence is in equilibrium i.e. mathematically

$$i_{\text{net}} = i_{df} + i_{dr} = 0$$

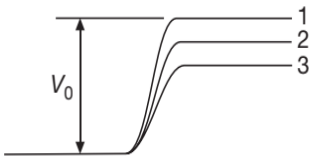
p-n JUNCTION DIODE UNDER FORWARD BIAS

When an external voltage V is applied across a semiconductor diode (having barrier potential V_B) such that *p*-side is connected to the positive terminal of the battery and *n*-side to the negative terminal of the battery, as shown in Figure, it is said to be *Forward Biased*.



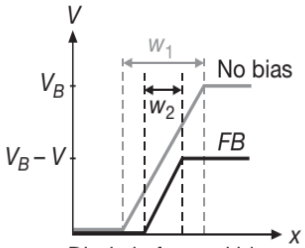
p-n junction diode under forward bias

The applied voltage mostly drops across the depletion region and the voltage drop across the *p*-side and *n*-side of the junction is negligible. This is because the resistance of the depletion region (a region where there are no charges) is very high compared to the resistance of *n*-side and *p*-side. The direction of the applied voltage (V) is opposite to that of the barrier potential (V_B). As a result, the depletion layer width decreases and the barrier height is reduced as shown in Figure.



Barrier potential (1) Without battery
(2) Low battery voltage, and
(3) High voltage battery

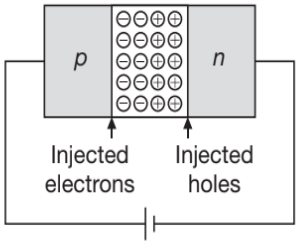
The effective barrier height under forward bias is $|V_B - V|$. As the applied voltage V is increased, the barrier potential decreases and width of depletion region also decreases.



Diode in forward bias
Width of depletion region is w_1 without bias and w_2 in forward bias ($w_2 < w_1$)

When the applied voltage is small, the barrier potential will be reduced only slightly below the equilibrium value, and only a small number of carriers in the material (only the ones which happen to be in the uppermost energy levels) will possess enough energy to cross the junction. Hence, the current will be small. However, when the applied voltage is significantly increased, then the barrier height will be reduced and more number of charge carriers will possess energy to cross the junction and hence the current increases.

Due to the applied voltage, the electrons from *n*-side cross the depletion region to reach the *p*-side (where they are minority carries). Similarly, holes from *p*-side cross the junction and reach the *n*-side (where they are minority carries). *This process under forward bias is called as minority carrier injection*. So, on each side of the junction boundary, the minority charge carrier concentration increases significantly compared to the locations that are far from the junction. Due to this concentration gradient, the injected electrons on *p*-side diffuse from the junction edge of *p*-side to the other end of *p*-side. Similarly, the injected holes on *n*-side diffuse from the junction edge of *n*-side to the other end of *n* -side (shown in figure).



Forward bias minority carrier injection

Hence a current is obtained due to this motion of the charge carriers. *The total diode forward current is sum of hole diffusion current and conventional current due to electron diffusion*. The magnitude of this forward current is usually in mA.

Conceptual Note(s)

When the junction diode is in forward bias, then

(a) width of depletion layer decreases.

(b) forward biasing resistance offered is

$R_{\text{Forward}} \approx 10\ \Omega - 25\ \Omega$

(c) forward bias opposes the potential barrier and for $V > V_B$, a forward current is set up across the junction.

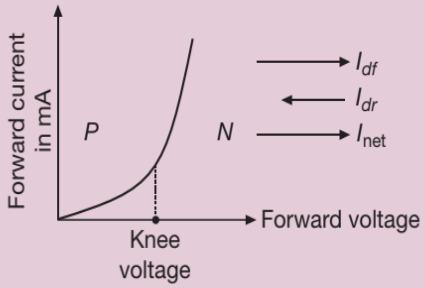
(d) the current is given by $i = i_s\left[\exp\left(\frac{eV}{k_BT}\right) - 1\right]$

where, i_s is the saturation current, $e = 1.6 \times 10^{-19}$ C, k_B is the Boltzmann's constant, V is the applied voltage and T is the absolute temperature.

(e) the cut-in voltage (also called as knee voltage) is the voltage at which the current starts to increase rapidily.

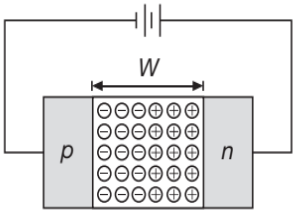
For Ge it is 0.3 V and for Si it is 0.7 V.

(f)



p-n JUNCTION DIODE UNDER REVERSE BIAS

When an external voltage V is applied across the diode such that n-side is connected to positive of the battery and p-side is connected to the negative of the battery, then the diode is said to be *Reverse Biased* as shown in Figure.

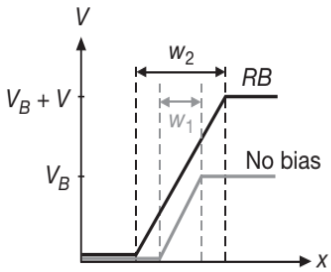


Diode under reverse bias

The applied voltage mostly drops across the depletion region. The nature of the applied voltage is same as the nature of barrier potential or we can say that the applied voltage helps the barrier potential. As a result of this, the barrier height increases and the depletion region widens due to the change in the electric field as shown in Figure.

Barrier potential under reverse bias

The effective barrier height under reverse bias is $(V_B + V)$. As the applied voltage V is increased, the barrier potential increases and width of depletion region also inceases.



Diode in reverse bias

Width of depletion region is w_1 without bias and w_2 in reverse bias ($w_2 > w_1$)

Due to this increased height of the barrier potential, the flow of electrons from $n \to p$ and holes from $p \to n$ region is suppressed. Thus, diffusion current, decreases enormously compared to the diode under forward bias.

The electric field direction at the junction is such that whenever the electrons on p-side or holes on n-side, in their random motion, come close to the junction, then they are swept to its majority zone. This drift of carriers gives rise to current called drift current which is of the order of a few μA. This is very low because this current is due to the motion of carriers from the minority side to the majority side across the junction. The drift current is also there under forward bias but it is negligible (μA) when compared with current due to injected carriers which is usually in mA.

Conceptual Note(s)

When the junction diode is in reverse bias, then

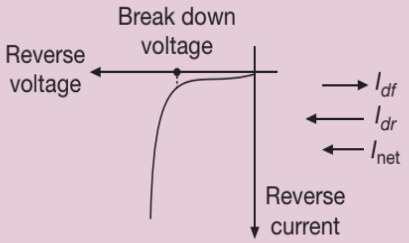
(a) width of depletion layer increases

(b) reverse biasing resistance offered is $R_{Reverse} \approx 10^5\ \Omega$

(c) reverse bias supports the potential barrier and no current flows across the junction due to the diffusion of the majority carriers. (A very small reverse currents may exist in the circuit due to the drifting of minority carriers across the junction)

(d) the break down voltage (also called Reverse voltage) is the voltage at which break down of semiconductor occurs.
For *Ge* it is 25 V and for *Si* it is 35 V.

(e)

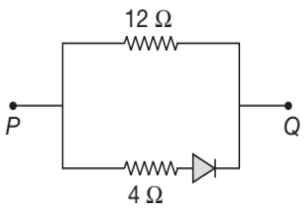


(f) The diode reverse current is not very much dependent on the applied voltage. Even a small voltage is sufficient enough to sweep the minority charge carriers from one side of the junction to the other side of the junction. So, the reverse current is not limited by the magnitude of the applied voltage but is limited because of the small concentration of the minority charge carriers on either side of the junction.

ILLUSTRATION 10

Calculate the net resistance of the network shown in the figure between the points P and Q when

(i) $V_P > V_Q$ **(ii)** $V_P < V_Q$



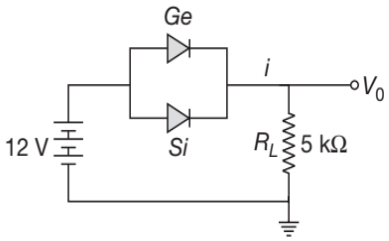
SOLUTION

(i) When $V_P > V_Q$, the diode is forward biased. Hence, the resistance of diode will be taken as zero. So, the net resistance is $\dfrac{4\times12}{4+12}\ \Omega = 3\ \Omega$.

(ii) When $V_P < V_Q$, the diode is reverse biased. Hence, there will be no current in the diode branch. So, the net resistance is $12\ \Omega$.

ILLUSTRATION 11

Calculate the value of V_0 and i if the silicon and germanium diode start conducting at 0.7 V and 0.3 V, respectively. If the *Ge* diode connection is now reversed, what will be the new values of V_0 and i?



SOLUTION

Here we must note that the germanium diode will start conducting before the silicon diode starts conducting. The effective forward voltage across the germanium diode is given by

$$V_0 = (12 - 0.3)\ \text{V} = 11.7\ \text{V}$$

This will appear as the output voltage across the load i.e.,

$$V_0 = 11.7\ \text{V}$$

So, the current through load resistance R_L is given by

$$i = \frac{11.7}{5\times10^3}\ \text{A} = 2.34\ \text{mA}$$

On reversing the connection of germanium diode, it will be reverse biased and will not conduct. So, only the silicon diode will conduct and then the output voltage across the laod is

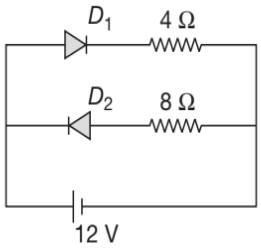
$$V_0 = (12 - 0.7)\ \text{V} = 11.3\ \text{volt}$$

So, the current through load resistance R_L is given by

$$i = \frac{11.3}{5\times10^3}\ \text{A} = 2.26\ \text{mA}$$

ILLUSTRATION 12

Calculate the current passing through the $4\ \Omega$ and $8\ \Omega$ resistors in the circuit shown in Figure.



SOLUTION

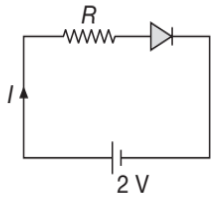
In the given circuit, diode D_1 is forward biased and D_2 is reverse biased. Hence, D_1 will conduct but D_2 will not.

Therefore, current through $8\ \Omega$ resistance will be zero whereas the current through $4\ \Omega$ resistance will be

$$I_{4\,\Omega} = \frac{12}{4} = 3\ \text{A}$$

ILLUSTRATION 13

The diode used in the circuit shown in the figure has a constant voltage drop of $0.5\ \text{V}$ at all current and a maximum power rating of $200\ \text{mW}$. What should be the value of the resistor R, connected in series with the diode, for obtaining maximum current?



SOLUTION

Current through diode (or circuit) is given by

$$I = \frac{\text{Power}}{\text{Voltage}}$$

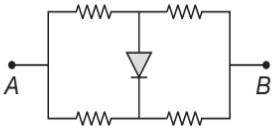
$$\Rightarrow \quad I = \frac{200\times10^{-3}\ \text{W}}{0.5\ \text{V}} = 0.4\ \text{A}$$

$$\text{Since, } R = \frac{\Delta V}{\Delta I} = \frac{\text{Net voltage}}{\text{Current}}$$

$$\Rightarrow \quad R = \frac{2-0.5}{0.4} = 3.75\ \Omega$$

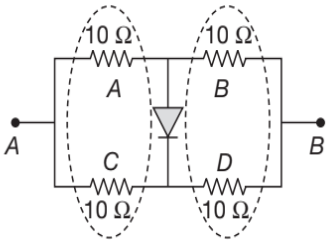
ILLUSTRATION 14

Calculate the net resistance between two points A and B, if the value of each resistance shown in the Figure is $10\ \Omega$.



SOLUTION

The given circuit is in the form of a wheatstone bridge.



Since we observe that

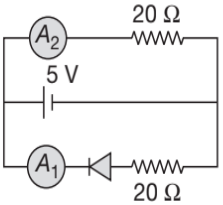
$$\frac{P}{Q} = \frac{R}{S}$$

Hence no current will from through the diode and hence it will not offer any resistance. So, the net resistance between A and B will be

$$R_{AB} = \frac{(10)(10)}{10+10} + \frac{(10)(10)}{10+10} = 20\ \Omega$$

ILLUSTRATION 15

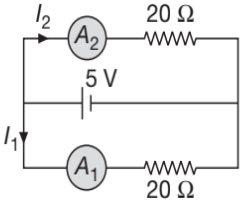
Two ammeters A_1 and A_2 are connected across a diode and resistor respectively as shown in the Figure.



Calculate the amount of current flowing through these two ammeters. Ignore the resistances of the meters.

SOLUTION

Let ae current I_1 flows across a diode and I_2 flows across a resistor as shown in the Figure.



Since the diode is in reverse biased condition, so it will not conduct. Hence, ammeter A_1 will not show any reading.

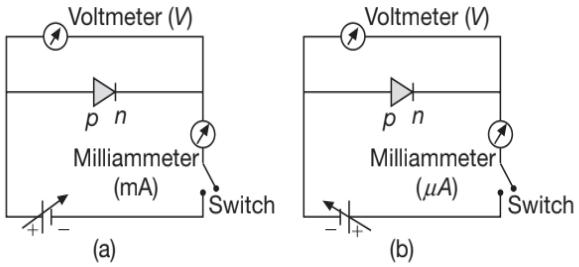
So, the ammeter A_2 will show a reading I_2 given by

$$I_2 = \frac{V}{R} = \frac{5}{20} = 0.25 \text{ A}$$

V-I CHARACTERISTICS OF A *p-n* JUNCTION DIODE

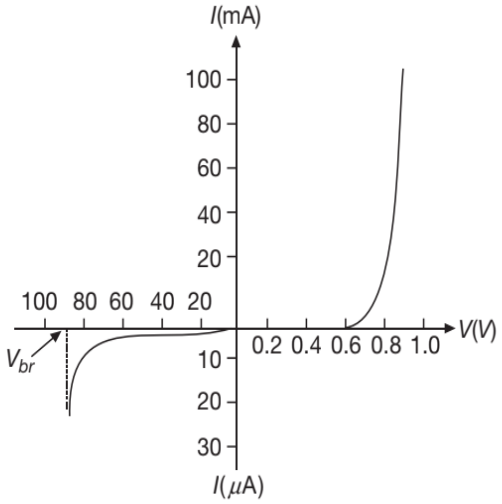
The current under reverse bias is essentially voltage independent upto a critical reverse bias voltage, known as breakdown voltage (V_{br}). When $V = V_{br}$, the diode reverse current increases sharply. Even a slight increase in the bias voltage causes large change in the current. If the reverse current is not limited by an external circuit below the rated value (specified by the manufacturer) the *p-n* junction will get destroyed. Once it exceeds the rated value, the diode gets destroyed due to overheating. This can happen even for the diode under forward bias, if the forward current exceeds the rated value.

The circuit arrangement for studying the *V-I* characteristics of a diode, (i.e., the variation of current as a function of applied voltage) are shown in figure.



The battery is connected to the diode through a potentiometer (or rheostat) so that the applied voltage to the diode can be changed. Note that in forward bias measurement, we use a milliammeter since the expected current is large (as explained in the earlier section) while a microammeter is used in reverse bias to measure the current.

For different values of voltages, the value of the current is noted. A graph between V and I is obtained as in Figure.



Experimental circuit arrangement for studying V-I characteristics of a *p-n* junction diode (a) in forward bias, (b) in reverse bias. (c) Typical V-I characteristics of a silicon diode.

We observe from the graph that in forward bias, the current first increases very slowly, almost negligibly, till the voltage across the diode crosses a certain value. After the characteristic voltage, the diode current increases significantly (exponentially), even for a very small increase in the diode bias voltage. *This voltage is called the Threshold Voltage or Cut-In Voltage or Knee Voltage* (≈ 0.3 V for germanium diode and ≈ 0.7 V for silicon diode).

The above discussion shows that the *p-n* junction diode primarily allows the flow of current only in one direction (forward bias). The forward bias resistance is low as compared to the reverse bias resistance.

DYNAMIC RESISTANCE OF A DIODE

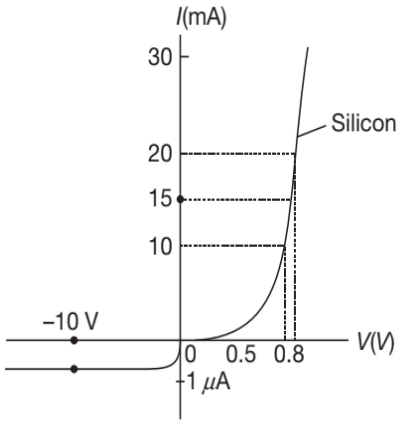
It is observed that both the forward bias and the reverse bias characteristics of the diode do not obey Ohm's Law, because the resistance offered by the junction diode depends on the applied voltage. Therefore, for diodes, we define a quantity called *dynamic resistance* (r_d) which is the ratio of small change in voltage ΔV to a small change in current ΔI. Mathematically

$$r_d = \frac{\Delta V}{\Delta I}$$

The region of the *V-I* graph where the dynamic resistance is almost independent of the applied voltage is called the linear region of the junction diode.

ILLUSTRATION 16

The V-I characteristic of a silicon diode is shown in Figure. Calculate the resistance of the diode at $I = 15$ mA and at $V = -10$ V.



SOLUTION

As seen from the figure, the diode current varies linearly between 10 mA to 20 mA. So, we can calculate the resistance using Ohm's law. From the curve, we observe that at $I = 20$ mA, $V = 0.8$ V and at $I = 10$ mA, $V = 0.7$ V. So, the forward bias resistace R_{fb} of the diode is

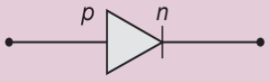
$$R_{fb} = \frac{\Delta V}{\Delta I} = \frac{0.1 \text{ V}}{10 \text{ mA}} = 10\ \Omega$$

From the curve, we see that at $V = -10$ V, $I = -1\ \mu$A. So, the reverse bias resistance R_{rb} of the diode is

$$R_{rb} = \frac{10 \text{ V}}{1\ \mu\text{A}} = 1 \times 10^7\ \Omega$$

Conceptual Note(s)

(a) the junction diode is represented by the symbol as shown in figure.

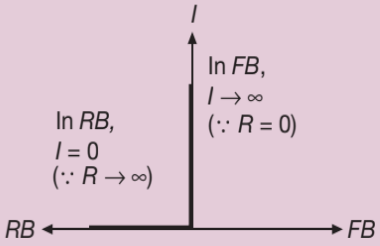


The arrow-head represents the p section of the junction diode and points in the direction in which the hole current or conventional current will flow, when junction diode is forward biased. The electron current or the electronic current will flow in opposite direction.

(b) It may be noted that the potential barrier opposes the forward current, while it aids the reverse current.

(c) The depletion region becomes thick and junction diode offers high resistance to current during Reverse bias.

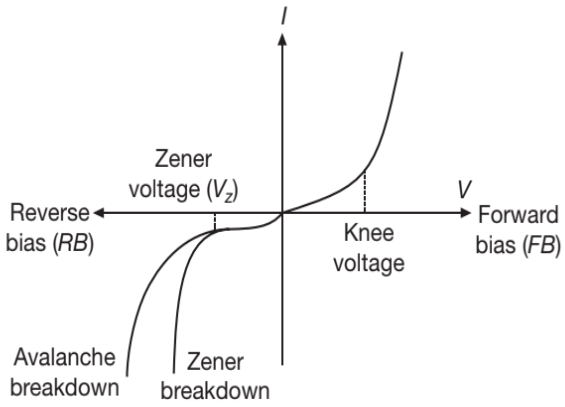
(d) For an ideal diode, the V-I relation is shown in figure. In forward bias (FB) of an ideal diode, $R = 0$ and hence $I \to \infty$. Similarly, in reverse bias (RB) of an ideal diode, $R \to \infty$ and hence $I = 0$.



(e) In practice, a *Ge* junction diode is preferred to *Si* junction diode. It is because, in case of *Ge* junction diode, the knee voltage is low (≈ 0.3 V) in comparison to that of *Si* junction diode (≈ 0.7 V).

ZENER AND AVALANCHE BREAKDOWN IN REVERSE BIAS OF A DIODE

For the diode in reverse bias, the current is very small $(\approx \mu\text{A})$ and almost remains constant with change in the bias. *It is called reverse saturation current*. However, for special cases, at very high reverse bias (break down voltage), the current suddenly increases. Depending upon the doping of the pn junction, we categorise the breakdown process in two categories.



Zener Breakdown

This breakdown occurs in a highly doped pn junction in which width of depletion region is small. When reverse bias voltage is increased, the electric field across depletion region also increases (which is the

sum of barrier electric field and applied electric field) and if we go on increasing the reverse bias voltage, then at a particular value of reverse voltage (called Zener voltage V_Z) a large number of electrons and holes are produced. This is called as *Zener Breakdown*.

AVALANCHE BREAKDOWN

This kind of breakdown occurs in a reverse bias of lightly doped *pn* junction. When the *pn* junction is lightly doped, then the width of depletion region is large. So, on increasing the reverse bias, some covalent bonds are broken in the depletion region and electron-hole pairs are produced, which further collide with atoms thus producing more electron-hole pairs. This results in a continuous flow of current carriers in reverse bias and these newly generated charge carriers are also accelerated by applied electric field in reverse bias thus leading to *Avalanche Breakdown*.

Conceptual Note(s)

Note that Zener breakdown predominates at lower reverse voltages and Avalanche breakdown at higher reverse voltages.

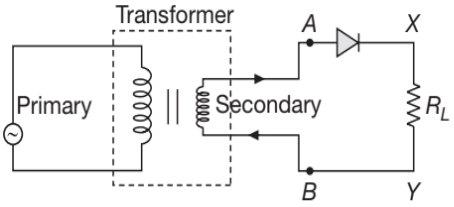
APPLICATION OF JUNCTION DIODE AS A RECTIFIER

From the V-I characteristic of a junction diode we see that it allows current to pass only when it is forward biased. So, if an alternating voltage is applied across a diode the current flows only in that part of the cycle when the diode is forward biased. This property is used to rectify alternating voltages and the circuit used for this purpose is called a rectifier.

Rectification process is the process of converting AC to DC. This is based on the principle that a diode conducts in FORWARD BIAS and a diode does not conduct in REVERSE BIAS.

Half Wave Rectifier (HWR)

If an alternating voltage is applied across a diode in series with a load, a pulsating voltage will appear across the load only during the half cycles of the ac input during which the diode is forward biased. Such a rectifier circuit is called a Half Wave Rectifier as shown in figure.

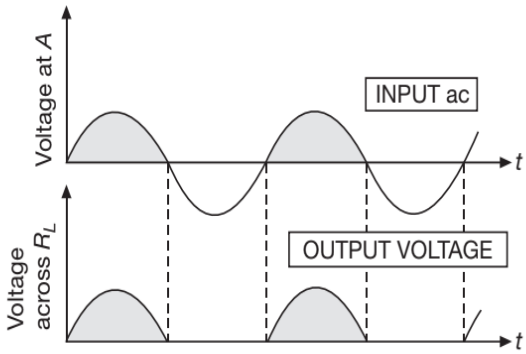


Half-wave rectifier circuit

The secondary of a transformer supplies the desired ac voltage across terminals A and B.
When the voltage at A is positive, then the diode is forward biased and it conducts.
When the voltage at A is negative, then the diode is reverse biased and it does not conduct.

The reverse saturation current of a diode is negligible and can be considered equal to zero for practical purposes. (The reverse breakdown voltage of the diode must be sufficiently higher than the peak ac voltage at the secondary of the transformer to protect the diode from reverse breakdown).

Therefore, for the positive half cycle of AC, there is a current through the load resistor R_L and we get an output voltage, as shown in Figure. However, there is no current flowing through the load resistor R_L for the negative half cycle.



Input ac voltage and output voltage waveforms from the rectifier circuit.

Now, for the next positive half cycle, again we get an output across the load resistance. So, we conclude that the output voltage, though still varying, is restricted only to one direction and hence is said to be rectified. Since the rectified output of this circuit is only for half of the input ac wave, so it is called as half wave rectifier (HWR).

Problem Solving Technique(s)

(a) Output voltage is obtained across the load resistance R_L. It is not constant but pulsating (mixture of ac and dc) in nature.

(b) The ripple frequency for half wave rectifier is same as that of ac, that is $\omega_{ripple} = \omega$.

(c) Average output in one cycle is

$$I_{dc} = \frac{I_0}{\pi} \text{ and } V_{dc} = \frac{V_0}{\pi}$$

where $I_0 = \dfrac{V_0}{r_f + R_L}$

where r_f is the forward resistance of the diode or the resistance of the diode in forward bias.

(d) Similarly, the r.m.s. output is

$$I_{rms} = \frac{I_0}{2} \text{ and } V_{rms} = \frac{V_0}{2}$$

(e) Form factor of the diode is the ratio of the rms current to the dc current. So, it is given by

$$\frac{I_{rms}}{I_{dc}} = \frac{\pi}{2} = 1.57$$

(f) The ratio of the effective alternating component of the output voltage or current to the dc component is known as Ripple factor (r).

$$r = \frac{I_{ac}}{I_{dc}} = \left(\left(\frac{I_{rms}}{I_{dc}} \right)^2 - 1 \right)^{1/2} = 1.21$$

(g) Peak inverse voltage (PIV) is the maximum reverse biased voltage that can be applied before commencement of Zener region. When diode is not conducting, then PIV across HWR is V_0.

(h) Efficiency of the diode is the ratio of the ouput power of the diode to the input power. The percentage efficiency η for HWR is given by

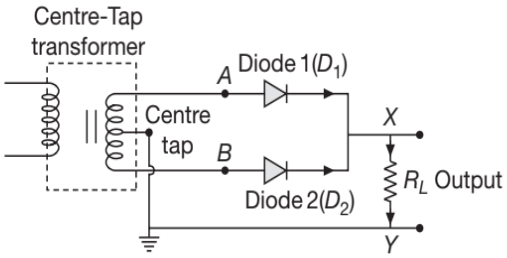
$$\eta_{HWR} = \frac{P_{out}}{P_{in}} \times 100\% = \left(\frac{40.6}{1 + \dfrac{r_f}{R_L}} \right)\%$$

If $R_L \gg r_f$, then $\eta_{HWR} = 40.6\%$

If $R_L = r_f$, then $\eta_{HWR} = 20.3\%$

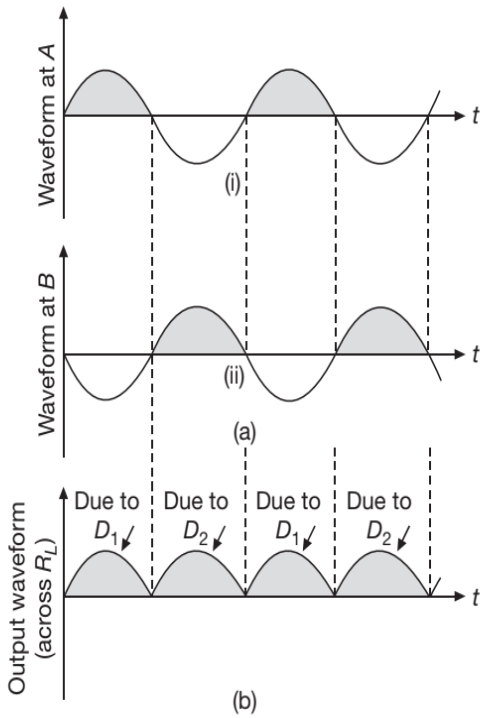
Full Wave Rectifier (FWR)

A FWR rectifies both halves of the ac input and it consists of two diodes. Since it gives a rectified output voltage for both the positive as well as negative half of the ac cycle, hence it is known as full wave rectifier (FWR). In FWR, the p side of each of the two diodes are connected to the ends of the secondary of the transformer as shown in figure.



A full-wave rectifier circuit

Similarly, the n side of both the diodes are connected together and then the output is taken between this common point of the diodes and the midpoint of the secondary of the transformer. So, for a full-wave rectifier, central tapping is done across the secondary of the transformer and hence it is called a Centrally Tapped Transformer. As can be seen from figure (b) atotal secondary voltage.



(a) Input wave forms given to the diode D_1 at A and to the diode D_2 at B; (b) Output waveform across the load R_L connected in the full-wave rectifier circuit.

For the course of ac input, when the input voltage at A (at any instant) is positive with respect to the centre tapping, then at that same instant, the voltage at B (being out of phase) will be negative. Hence diode D_1 gets forward biased and conducts whereas, diode D_2 get reversed bias and does not conduct. So, for this positive half input cycle, we get an output current and an output voltage across the load resistor R_L.

Similarly, for the next half of the ac input, the voltage at A becomes negative with respect to central tapping, then the voltage at B would be positive. For this part of the cycle, we observe that the diode D_1 does not conducts, but the diode D_2 conducts so that an output current and output voltage is obtained across the load resistance R_L.

So, we get an output voltage both during positive as well as the negative half of the ac input. It is quite clear that this (FWR) is a more efficient circuit for getting rectified voltage or current compared to HWR.

Please note that each diode rectifies only for half the cycle, but the two do so for alternate cycles. Thus, the output between the common terminals of the diode and the centrally tapped transformer becomes a full wave rectifier output.

Problem Solving Technique(s)

(a) Output voltage is obtained across the load resistance R_L. It is not constant but pulsating (mixture of ac and dc) in nature.

(b) The ripple frequency for full wave rectifier is twice the input frequency of the ac, hence $\omega_{ripple} = 2\omega$

(c) Average output in one cycle is

$$I_{dc} = \frac{2I_0}{\pi} \text{ and } V_{dc} = \frac{2V_0}{\pi},$$

where $I_0 = \dfrac{V_0}{r_f + R_L}$

where r_f is the forward resistance of the diode or the resistance of the diode in forward bias.

(d) Similarly, the r.m.s. output is

$$I_{rms} = \frac{I_0}{\sqrt{2}} \text{ and } V_{rms} = \frac{V_0}{\sqrt{2}}$$

(e) Form factor of the diode is the ratio of the rms current to the dc current. So, it is given by

$$\frac{I_{rms}}{I_{dc}} = \frac{\pi}{2\sqrt{2}} = 1.11$$

(f) The ratio of the effective alternating component of the output voltage or current to the dc component is known as Ripple factor (r).

$$r = \frac{I_{ac}}{I_{dc}} = \left[\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1\right]^{1/2} = 0.48$$

(g) Peak inverse voltage (PIV) is the maximum reverse biased voltage that can be applied before commencement of Zener region. When diode is not conducting, then PIV across FWR is $2V_0$.

(h) Efficiency of the diode is the ratio of the ouput power of the diode to the input power. The percentage efficiency η for FWR is given by

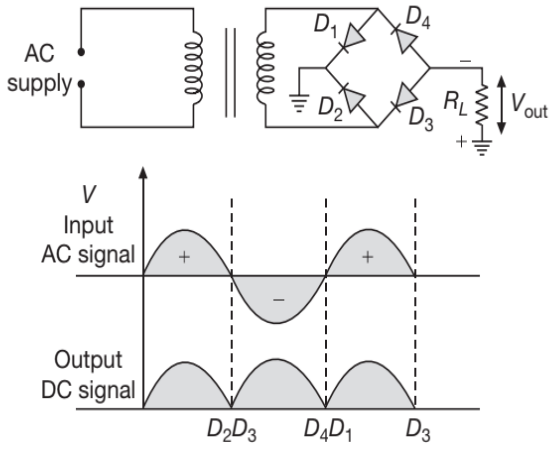
$$\eta_{FWR} = \frac{P_{out}}{P_{in}} \times 100\% = \left(\frac{81.2}{1 + \dfrac{r_f}{R_L}}\right)\%$$

If $R_L \gg r_f$, then $\eta_{FWR} = 81.2\%$

If $R_L = r_f$, then $\eta_{FWR} = 40.6\%$

Full Wave Bridge Rectifier

There is another circuit of full wave rectifier which does not need a centrally tapped transformer but needs four diodes D_1, D_2, D_3 and D_4 as shown in figure.



During positive half cycle D_1 and D_3 are forward biased and D_2 and D_4 are reverse biased. During negative half cycle D_2 and D_4 are forward biased and D_1 and D_3 are reverse biased

FILTER CIRCUITS

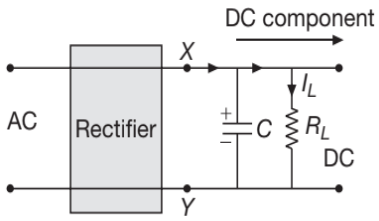
The rectified voltage is in the form of pulses of the shape of half sinusoids. Though the output is unidirectional, still it does not have a steady value.

To get a steady dc output from the pulsating voltage, normally a capacitor is connected across the output terminals (parallel to the load resistance R_L). We can also use an inductor in series with the load resistance R_L for the same purpose. Since these additional circuits appear to filter out the AC ripple and give a pure DC voltage, so they are called as Filters.

Fluctuating DC → Filter → Constant DC

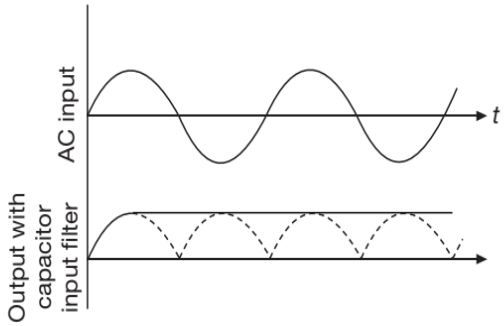
Role of Capacitor in Filter Circuits

When the capacitor is connected across the output terminals in parallel to the load resistance R_L, then a steady dc output from the pulsating voltage can be obtained.



A full-wave rectifier with capacitor filter

When the voltage across the capacitor is rising, it gets charged. If there is no external load, then the capacitor remains charged to the peak voltage of the rectified output. However, when there is a load, the capacitor gets discharged through the load and the voltage across it begins to fall. In the next half cycle of the rectified output, the capacitor again gets charged to the peak value. The rate of fall of the voltage across the capacitor is inversely proportional to the capacitive time constant R_LC of the circuit (i.e. the product of capacitance C of the capacitor and the effective resistance R_L used in the circuit). To make the capacitive time constant large, the value of C should also be large. It is because of this reason, the capacitor input filters make use of capacitor having large capacitances. The output voltage obtained by using capacitor input filter is very close to the peak voltage of the rectified output. This type of filter is most widely used in power supplies.



Input and output voltage of FWR

ILLUSTRATION 17

In a full-wave rectifier circuit operating from 100 Hz mains frequency, what is the fundamental frequency in the ripple?

SOLUTION

In a full wave rectification process, the output signal (ripple) frequency is double that of input signal frequency. Hence, output frequency is 200 Hz.

ILLUSTRATION 18

The applied input ac to a half wave rectifier is 60 W. The dc output is 20 W. Calculate the rectification efficiency. Also calculate the value of power efficiency.

SOLUTION

Rectification efficiency (η_R) is the ratio of dc output power to the ac input power, so rectification efficiency

$$\eta_R = \frac{DC \text{ output power}}{AC \text{ input power}}$$

Given that dc output power $P_{dc} = 20$ W

and ac input power $P_{ac} = 60$ W

$$\Rightarrow \quad \eta_R = \frac{20}{60} \times 100 = 33.3\%$$

The power efficiency (η_P) of a rectifier is given by

$$\eta_P = \frac{DC \text{ output power}}{AC \text{ input power for half cycle}} \times 100\%$$

$$\Rightarrow \quad \eta_P = \frac{20}{30} \times 100\% = 66.67\%$$

ILLUSTRATION 19

In a centrally tapped full wave rectifier, the value of the load resistance is 2 kΩ. The voltage applied across the half the secondary winding is given by

$V = 220\sin(314t)$. Assume that the each diode has a forward bias dynamic resistance of $20\ \Omega$. Calculate the peak value of current, the dc value of current and the rms value of current.

SOLUTION

Comparing $V = 220\sin(314t)$ with the general equation $V = V_0\sin(\omega t)$, we get $V_0 = 220$ V and $\omega = 314$ rads^{-1}

Also, it is given that $R_L = 2\ \text{k}\Omega$, $r_d = 20\ \Omega$

Peak value of current is

$$I_0 = \frac{V_0}{(r_d + R_L)} = \frac{220}{20 + 2000} \approx 109\ \text{mA}$$

dc value of current is

$$I_{dc} = \frac{2I_0}{\pi} = \frac{2\times 109}{3.14} = 69.4\ \text{mA}$$

RMS value of current is

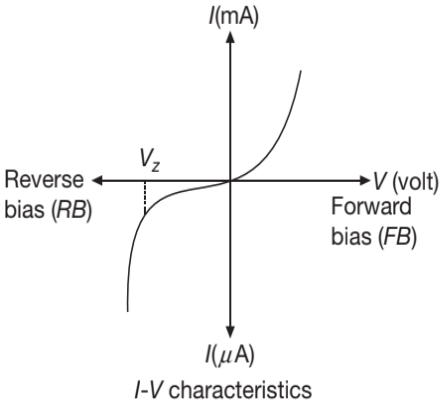
$$I_{\text{rms}} = \frac{I_0}{\sqrt{2}} = 0.707\times 109 = 77.06\ \text{mA}$$

ZENER DIODE: SPECIAL PURPOSE JUNCTION DIODE

Zener diode is actually a junction diode developed for a special purpose. It is named after its inventor Clarence Melvin Zener. This diode is designed to operate under reverse bias in the breakdown region and is used as a voltage regulator. Zener diodes have highly doped *pn*-junction. Normally diodes are not designed to operate in the breakdown region, however Zener diodes operate reliably in this region. The symbol for Zener diode is shown in figure.

Zener diode symbol

Due to the heavy doping of both the *p* side and the *n* side of the junction, the depletion region formed is very thin $(<10^{-6}\ \text{m})$ and hence the electric field of the junction is extremely high $(\approx 5\times 10^{6}\ \text{Vm}^{-1})$ even for a small reverse bias voltage of about 5 V. The *I-V* characteristics of a Zener diode is shown in figure.



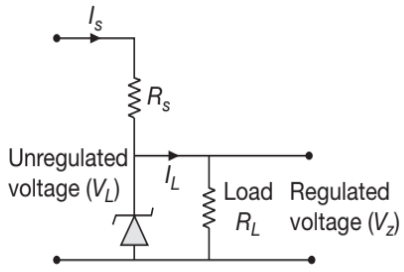
I-V characteristics

It is observed that when the applied reverse bias voltage (V) reaches the breakdown voltage (V_z) of the Zener diode, then there is a large change in the current. Also, it is observed that after the breakdown voltage V_z, a large change in the current can be produced by almost insignificant change in the reverse bias voltage. *In other words, Zener voltage remains constant, even though current through the Zener diode varies over a wide range.* This property of the Zener diode is used for regulating supply voltages so that they are constant.

Let us understand how reverse current suddenly increases at the breakdown voltage. We know that reverse current is due to the flow of electrons (minority carriers) from $p \to n$ and holes from $n \to p$. As the reverse bias voltage is increased, the electric field at the junction becomes significant. When the reverse bias voltage V equals the Zener voltage V_z, then the electric field strength is high enough to pull the valence electrons from the host atoms on the *p*-side which are then accelerated to *n*-side. These electrons account for high current observed at the breakdown. *The emission of electrons from the host atoms due to the high electric field is known as internal field emission or field ionisation.*

ZENER DIODE AS A VOLTAGE REGULATOR

The most important use of Zener diode is that it can be used as voltage regulator. When the ac input voltage of a rectifier fluctuates, its rectified output also fluctuates. To get a constant dc voltage from the dc unregulated output of a rectifier, we use a Zener diode. The circuit diagram of a voltage regulator using a Zener diode is shown in figure.



Zener diode as DC voltage regulator

The regulating action takes place because in the reverse breakdown region, a very small change in voltage produces a very large change in current. In the Zener region, the resistance of the Zener diode drops considerably (due to the large current). The unregulated dc voltage (filtered output of a rectifier) is connected to the Zener diode through a series resistance R_s such that the Zener diode is reverse biased.

As the input voltage increases, the current through R_S and Zener diode also increases. This increases the voltage drop across R_S without any change in the voltage across the Zener diode (which still remains V_Z). This is because in the breakdown region, Zener voltage remains constant even though the current through the Zener diode changes.

Similarly, when the input voltage decreases, the current through R_S and Zener diode also decreases. The voltage drop across R_S decreases without any change in the voltage across the Zener diode (which still remains V_Z).

When the applied input voltage $\left(V_{\text{input}}\right)$ is such that the voltage across the Zener diode is less than the Zener voltage, then the diode will not conduct and the output voltage $\left(V_{\text{output}}\right)$ is given by

$$V_{\text{output}} = \left(\frac{R_L}{R_S + R_L}\right) V_{\text{input}}$$

However, when the applied input voltage is such that the voltage developed across the Zener diode is more that the Zener voltage $\left(V_Z\right)$, then the output voltage is equal to the Zener voltage i.e.

$$V_{\text{output}} = V_Z$$

Thus, any increase or decrease in the input voltage results in the corresponding increase or decrease of the voltage drop across R_s without any change in voltage across the Zener diode (which still remains V_Z). Due to this, the Zener diode acts as a voltage regulator. We have to select the Zener diode according to the required output voltage and according to the the series resistance R_S. *Every Zener diode has a certain value of current limit and the corresponding power limit. If the current in the Zener diode exceeds this limit, then the diode will burn.*

The graph of output voltage V_{output} vs input voltage V_{input} for the Zener diode is shown in Figure. It must be noted that the output voltage remains constant after the reverse breakdown voltage (i.e. Zener voltage V_Z) is obtained.

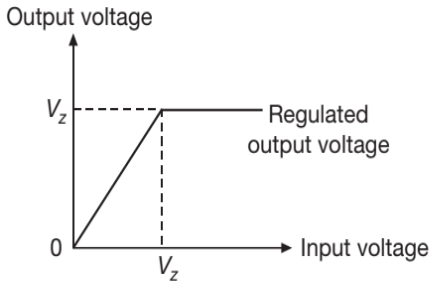


ILLUSTRATION 20

In a Zener regulated power supply a Zener diode with $V_Z = 6$ V is used for regulation. The load current is to be 4 mA and the unregulated input is 10 V. What should be the value of series resistor R_S? Assume that the Zener current is five times the load current.

SOLUTION

The value of R_S should be such that the current through the Zener diode is much larger than the load current. This is to have good load regulation. Since Zener current is five times the load current, so $I_Z = 20$ mA.

The total current through R_S is given by

$$I_S = I_Z + I_L = 24 \text{ mA}$$

The voltage drop across R_S is

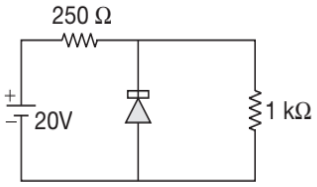
$$\Delta V_S = V_{\substack{\text{unregulated} \\ \text{input voltage}}} - V_Z = 10 - 6 = 4 \text{ V}.$$

$$\Rightarrow \quad R_S = \frac{\Delta V_S}{I_S} = \frac{4 \text{ V}}{24 \times 10^{-3} \text{ A}} = 167 \ \Omega$$

Note that slight variation in the value of the resistor does not matter, what is important is that the current I_Z should be sufficiently larger than I_L.

ILLUSTRATION 21

The breakdown voltage of a Zener diode is 12 V. It is used in a voltage regulator circuit shown in figure. Calculate the current through the diode.



SOLUTION

Current through 250 Ω resistor is

$$I_1 = \frac{\Delta V}{\Delta I} = \frac{(20-12)\text{ V}}{250\ \Omega}$$

$$\Rightarrow \quad I_1 = 32\times10^{-3}\text{ A} = 32\text{ mA}$$

Current through 1 kΩ resistor is

$$I_2 = \frac{12\text{ V}}{1\text{ k}\Omega} = 12\times10^{-3}\text{ A} = 12\text{ mA}$$

So, current through the Zener diode is

$$I_Z = I_1 - I_2 = 32\text{ mA} - 12\text{ mA} = 20\text{ mA}$$

OPTO ELECTRONIC JUNCTION DEVICES

Till now we have studied the behaviour of a semiconductor diode under the applied electrical inputs. However, there are semiconductor diodes in which charge carriers are generated by photons (i.e. by photo-excitation). *These types of diodes are called opto-electronic devices*. Let us study the functioning of the following optoelectronic devices

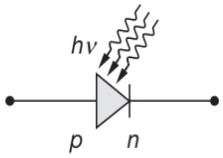
(i) Photodiodes: Which are used to detect optical signal and are also called as photodetectors.

(ii) Light Emitting Diodes (LED): Which converts an electrical energy into light.

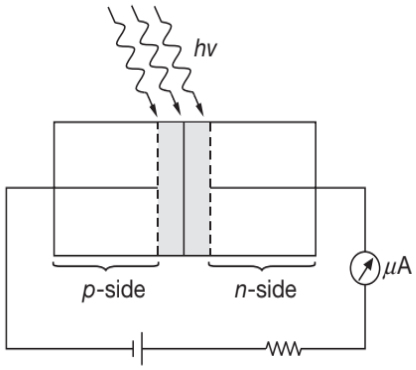
(iii) Photovoltaic devices: Which converts optical radiation into electricity also called as solar cells.

Photodiode

A photodiode is again a special purpose *p-n* junction diode which can be used as a photodetector to detect optical signals. Its symbolic representation is shown in figure.



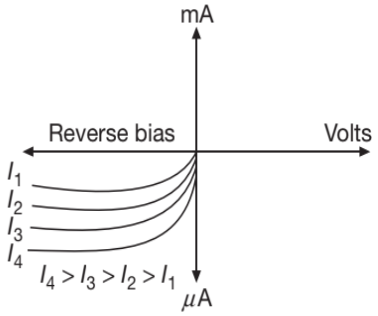
This diode is fabricated with a transparent window to allow light to fall on the diode. It is always operated in the reverse bias mode as shown in the Figure, where the circuit used to measure *I-V* characteristics of a photodiode is shown.



An illuminated photodiode under reverse bias.

When the photodiode is illuminated with light having photons of energy $h\nu$ greater than the forbidden energy gap (E_g) of the semiconductor, then electron-hole pairs are generated due to the absorption of photons. The diode is fabricated in such a manner that the generation of electron-hole pair takes place in or near the depletion region of the diode. Due to electric field of the junction, these electrons and holes get separated before they recombine. The direction of the electric field is such that electrons reach *n*-side and holes reach *p*-side of the junction, due to which an emf is setup across the junction. When an external load is connected across it, a current flow through the load. Since, photocurrent is proportional to the intensity of incident light, hence the magnitude of the photocurrent depends on the intensity light incident on the diode.

Please note that, if the diode is reverse biased, then it is easier to observe the change in the current with change in the light intensity. A typical *I-V* characteristic curve for the photodiode is shown in figure.



I-V characteristics of a photodiode for different illumination intensity $I_4 > I_3 > I_2 > I_1$

Conceptual Note(s)

The current in the forward bias is known to be more (≈ mA) than the current in the reverse bias (≈ μA), still we operate the diode in reverse bias. To explain the need to operate the photodiode in reverse bias mode, let us consider the case of an *n*-type semiconductor in which the charge density of majority carriers i.e. electrons is considerably larger than the charge density of minority carriers i.e. holes, so $n \gg p$, where n and p are respective electrons and holes concentration when there is no illumination. On illumination of the diode by a photon, let the excess electrons and holes generated be Δn and Δp respectively. If n' and p' be the electron and hole concentrations at any particular illumination, then we have

$$n' = n + \Delta n$$
$$p' = p + \Delta p$$

Since, $\Delta n = \Delta p$ and $n \gg p$, so the fractional change in the majority carriers i.e. $\frac{\Delta n}{n}$ would be much less compared to the fractional change in the minority carriers i.e. $\frac{\Delta p}{p}$.

Hence, we observe that, the fractional change due to the photo-effects on the minority carriers produces a larger reverse bias current which is more easily measurable than the fractional change in the forward bias current. Due to this, photodiodes are preferably used in the reverse bias condition for measuring light intensity.

ILLUSTRATION 22

A pn photodiode is made of a material with a band gap of 1.5 eV . Calculate the minimum wavelength of radiation that can be absorbed by the material.

SOLUTION

Since the energy of the photon is given by

$$E = h\nu = \frac{hc}{\lambda}$$

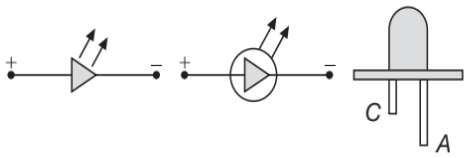
The minimum wavelength of radiation

$$\lambda = \frac{hc}{E} = \frac{(6.4\times10^{-34}\ \text{Js})\times(3\times10^{8}\ \text{ms}^{-1})}{1.5\times1.6\times10^{-19}\ \text{J}}$$

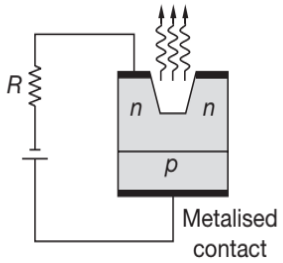
$$\Rightarrow \quad \lambda = 8.3\times10^{-7}\ \text{m} = 8300\ \text{Å}$$

Light Emitting Diode (LED)

LED is a heavily doped *p-n* junction which emits spontaneous radiation under forward bias. LED is encapsulated with a transparent cover so that emitted light can come out. The symbolic representation of LED and its actual shape is shown in Figure, where the longer terminal corresponds to the *p*-side and the shorter terminal corresponds to the *n*-side of the LED.



A *p-n* junction made from a translucent semiconductor like indium phosphide or gallium arsenide is provided with metal contacts as shown in figure.



A *p-n* junction made from a translucent semiconductor like gallium arsenide or indium phosphide is provided with metallised contacts, as shown in figure. When it is forward biased through a series resistance R, light photons are emitted from the non-metallised surface of the *n*-region. The series resistance R limits the current through the LED and hence controls the intensity of light emitted by it.

When this junction is forward biased through a resistor R connected in series to the diode, then photons are emitted from the non metallic surface of the *n*-region. The resistor R controls the current through the LED and hence controls the intensity of light emitted by the diode.

When the diode is forward biased, electrons are sent from *n*-region to the *p*-region (where they are minority carriers) and holes are sent from *p*-region to the *n*-region (where they are minority carriers). Close to the junction, the concentration of minority carriers increases compared to the equilibrium concentration (i.e., when there is no bias). So, on either side of the junction, excess minority carriers are there which recombine with majority carriers (near the junction). Due to recombination of charge carriers, the energy

is released in the form of photons. It is observed that photons with energy equal to or slightly less than the band gap or forbidden energy gap are emitted. When the forward current of the diode is small, the intensity of emitted light is small. As the forward current increases the intensity of emitted light increases and reaches a maximum. Further increase in the forward current results in decrease of light intensity. LEDs are biased such that the light emitting efficiency is maximum.

The V-I characteristics of a LED is similar to that of a Si junction diode. But the threshold voltages are much higher and slightly different for each colour. The reverse breakdown voltages of LEDs are very low, typically around $5\ V$. So, care should be taken that high reverse voltages do not appear across them.

LEDs that can emit red, yellow, orange, green and blue light are commercially available. The semiconductor used for fabrication of visible LEDs must at least have a band gap of $1.8\ eV$ (spectral range of visible light is from about $0.4\ \mu m$ to $0.7\ \mu m$, i.e., from about $3\ eV$ to $1.8\ eV$). The compound semiconductor Gallium Arsenide Phosphide $(GaAs_{1-x}P_x)$ is used for making LEDs of different colours. For making red LED, $GaAs_{0.6}P_{0.4}$ having $E_g \approx 1.9\ eV$ is used. For making infrared LED, $GaAs$ having $E_g \approx 1.4\ eV$ is used.

LEDs have the following advantages over conventional incandescent low power lamps.

(a) Low operational voltage and less power.
(b) Fast action and no warm-up time required.
(c) The bandwidth of emitted light is $100\ Å$ to $500\ Å$ or in other words it is nearly (but not exactly) monochromatic.
(d) Long life and ruggedness.
(e) Fast on-off switching capability.

These LEDs find extensive use in remote controls, burglar alarm systems, optical communication, etc. Extensive research is being done for developing white LEDs which can replace incandescent lamps.

ILLUSTRATION 23

A voltage drop of $2\ V$ occurs across a light emitting diode (LED) and a current of $10\ \mu A$ is passed through it when it is operated with a $6\ V$ battery having a limiting resistor R. Calculate the value of R.

SOLUTION

$$\text{Current, } I = \frac{\Delta V}{R}$$

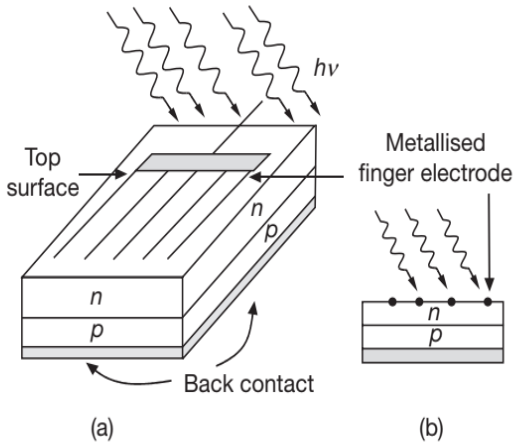
$$\Rightarrow \quad R = \frac{\Delta V}{I}$$

Resistance of limiting resistor will be

$$R = \frac{(6-2)\ V}{10 \times 10^{-6}\ A} = 400\ k\Omega$$

Solar Cell

A solar cell is basically a p-n junction which generates emf when solar radiation falls on the p-n junction. It works on the principle of photovoltaic effect (which is the process of generation of voltage due to bombardment of photons). The process is just similar as the photodiode, except that no external bias is applied and the junction area is kept much larger for solar radiation to be incident, so as to get more power. A simple p-n junction solar cell is shown in figure.



(a) Typical p-n junction solar cell; (b) Cross-sectional view

A p-type Silicon $(p\text{-}Si)$ wafer of about $300\ \mu m$ is taken, over which a thin layer $(\approx 0.3\ \mu m)$ of n-type Silicon $(n\text{-}Si)$ is grown on one side by the diffusion process. The other side of $p\text{-}Si$ is coated with a metal that forms the *back contact*. On the top of $n\text{-}Si$ layer, metal finger electrode also called as metallic grid is deposited. This acts as the *front contact*. The metallic grid occupies only a very small fraction of the cell area $(<15\%)$ so that light can be incident from the top on sufficiently large area of the cell.

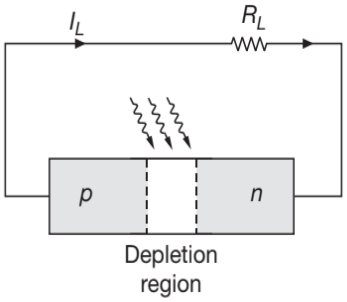
When light falls on a solar cell, the generation of emf is due to the following three basic processes

(a) Generation: In this process, the electron-hole pairs are generated (close to the junction) due to the falling light having $h\nu > E_g$.

(b) Separation: In this process, the separation of electrons and holes takes place due to electric field of the depletion region. The electrons are swept to *n*-side and holes to the *p*-side

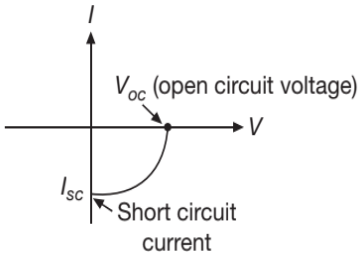
(c) Collection: In this process, the electrons reaching the *n*-side are collected by the front contact and holes reaching *p*-side are collected by the back contact. Due to this process, the *p*-side becomes positive and the *n*-side becomes negative, thus giving rise to a photovoltage.

When an external load is connected in the external circuit, as shown in the figure, a photocurrent I_L flows through the load resistor R_L. This current is proportional to the intensity of light falling on the cell.



A typical illuminated *p-n* junction solar cell

A typical I-V characteristics of a solar cell is shown in the figure.



I-V characteristics of a solar cell

Note that the I-V characteristics of solar cell is drawn in the fourth quadrant of the coordinate axes. This is because a solar cell does not draw current but supplies the same to the load.

Semiconductors with band gap close to 1.5 eV are ideal materials for solar cell fabrication. Solar cells are made with semiconductors like

Si having $E_g = 1.1$ eV,

GaAs having $E_g = 1.43$ eV

CdTe having $E_g = 1.45$ eV

$CuInSe_2$ having $E_g = 1.04$ eV etc.

The important criteria for the selection of a material for solar cell fabrication are

(a) band gap $(\approx 1$ to 1.8 eV$)$,
(b) high optical absorption $(\approx 10^4\ \text{cm}^{-1})$,
(c) electrical conductivity,
(d) availability of the raw material, and
(e) cost.

Solar cells are used to power electronic devices in satellites and space vehicles and also as power supply to some calculators. Rigorous research and efforts are going on for the production of low cost photovoltaic cells for large scale solar energy.

Conceptual Note(s)

Please note that sunlight is not always required for a solar cell. Any light with photon energies greater than the bandgap will do.

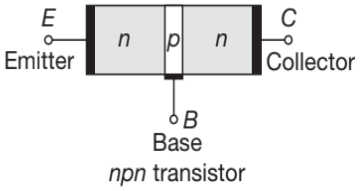
JUNCTION TRANSISTOR

Transistor (also called as Junction Transistor) was first invented by J Bardeen and WH Brattain of Bell Telephone Laboratories, USA. A junction transistor is a three terminal solid state device obtained by growing either a narrow section of *p*-type crystal between two relatively thicker sections of *n*-type crystals or a narrow section of *n*-type crystal between two thicker sections of *p*-type crystals. Transistors are mainly of two types

(a) npn transistor
(b) pnp transistor

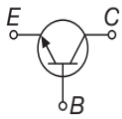
NPN Transistor

A *npn* transistor consists of a thin section of *p*-type semiconductor sandwiched between two thicker sections of *n*-type semiconductors as shown in figure.



npn transistor

The circuit symbol for the *npn* transistor is shown in Figure.

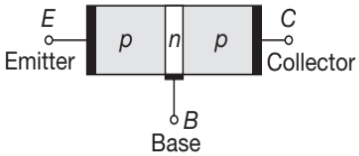


npn transistor symbol

Please note that, the arrowhead in the transistor symbol is shown in the base emitter branch and in the case of *npn* transistor the arrow is pointing from *p* to *n* i.e. from base to emitter.

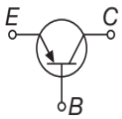
PNP Transistor

A *pnp* transistor consists of a thin section of *n*-type semiconductor sandwiched between two thicker sections of *p*-type semiconductors as shown in Figure.



pnp transistor

The circuit symbol for the *pnp* transistor is shown in Figure.



pnp transistor symbol

Here too, the arrowhead in the transistor symbol is shown in the base emitter branch and in the case of *pnp* transistor, the arrow is pointing from *p* to *n* i.e. from emitter to base. In both the types of transistors, the arrowhead at the emitter, points along the direction of conventional current.

Conceptual Note(s)

(a) A transistor can be compared with triode value. The Emitters can be compared to cathode of triode valve. The collector can be compared with the plate and the base with the grid of the Triode valve.

(b) Base is kept thin and is comparatively lightly doping.

(c) Symbol for transistors is always drawn keeping in mind to show the direction of conventional current in the Emitter-Base branch.

TRANSISTOR CONSTRUCTION

Each type of transistor has three main parts.

(a) The Emitter **(b)** The Base
(c) The Collector

Emitter (E)

The emitter is a section on one side of the transistor. It is a moderately sized and heavily doped semiconductor. It is normally forward biased w.r.t. any other part of the transistor. It supplies a large number of majority charge carriers for the flow of current through the transistor.

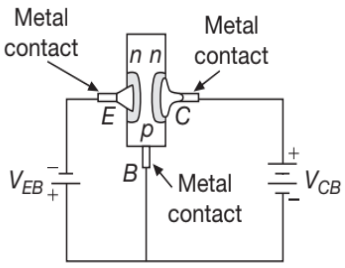
Base (B)

The base is the middle section of a transistor. It is very thin and lightly doped. It controls the flow of majority charge carriers from emitter to collector.

Collector (C)

The collector is a section on the other side of the transistor. It is larger in size and moderately doped as compared to the emitter. Normally it is reverse biased w.r.t. any other part of the transistor. It collects the majority charge carriers for the circuit operation.

The relative sizes of the three regions of the *npn* transistor and the biasing of base-emitter and base-collector junctions is shown in the Figure.



Relative sizes of the three regions of the *npn* transistor and the biasing

The forward bias voltage V_{EB} is small (0.5 V to 1 V) while the reverse bias voltage V_{CB} is high (5 V to 15 V).

WORKING OF TRANSISTOR

There are four possible ways of biasing the two *pn* junctions (emitter junction and collector junction) of transistor.

(a) **Cut-off mode:** Denotes operation like an open switch where only leakage current flows.
(b) **Active mode:** Also known as linear mode operation.
(c) **Inverse mode:** The emitter and collector are inter changed.
(d) **Saturation mode:** Maximum collector current flows and transistor acts as a closed switch from collector to emitter terminals.

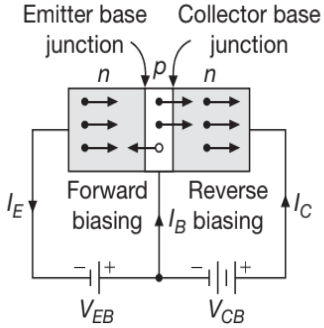
Table 4.1 Different modes of operation of a transistor

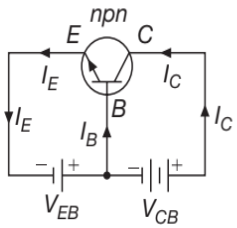
Operating mode	Emitter base bias	Collector base bias
Cut off	Reverse	Reverse
Active	Forward	Reverse
Inverse	Reverse	Forward
Saturation	Forward	Forward

A transistor is mostly used in the active region of operation i.e. emitter base junction is forward biased and collector base junction is reverse biased. From the operation of junction transistor, it is found that whenever the current in emitter circuit changes, then there is a corresponding change in the collector current. In each state of the transistor there is an input port and an output port. In general, each electrical quantity (V or I) obtained at the output is controlled by the input.

ACTION OF NPN TRANSISTOR

The emitter of the *npn* transistor is forward biased by connecting it to the negative terminal of the V_{EB} battery and the collector is reverse biased by connecting it to the positive terminal of the V_{CB} battery, as shown in Figure.





Action of *npn* transistor and its biasing

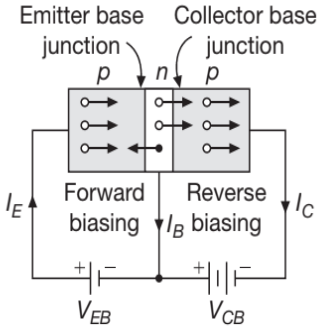
The forward bias of the emitter-base circuit repels the electrons of emitter towards the base, setting up emitter current I_E. As the base is very thin and lightly doped, a very few electrons $(< 5\%)$ from the emitter combine with the holes of base, giving rise to base current I_B and the remaining electrons $(> 95\%)$ are pulled by the collector which is at high positive potential. These electrons are finally collected by the positive terminal of V_{CB} battery, giving rise to collector current I_C. As soon as an electron from the emitter combines with a hole in the base region, an electron leaves the negative terminal of the V_{EB} battery and at the same time, the positive terminal of V_{EB} battery receives an electron from the base due to which a base current I_B is set up in the circuit. Similarly, corresponding to each electron that goes from collector to positive terminal of the V_{CB} battery, an electron enters the emitter from negative terminal of V_{EB} battery. Both the base current I_B and collector current I_C combine to form emitter current I_E, such that

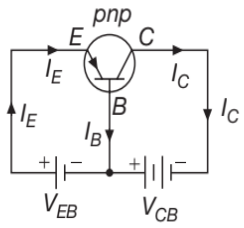
$$I_E = I_B + I_C$$

Here I_B is a small fraction of I_C i.e. $[I_B \ll I_C]$ depending on the shape of transistor, thickness of base, doping levels, bias voltages, etc.

ACTION OF PNP TRANSISTOR

The emitter of the *pnp* transistor is forward biased by connecting it to the positive terminal of V_{EB} battery and the collector is reverse biased by connecting it to the negative terminal of the V_{CB} battery, as shown in Figure.





Action of *pnp* transistor and its biasing

The forward bias of the emitter-base circuit repels the holes of emitter towards the base and electrons of base towards the emitter. As the base is very thin and lightly doped, most of the holes $(>95\%)$ entering it pass on to collector while a very few of them $(<5\%)$ recombine with the electrons of the base region. As soon as a hole combines with an electron, an electron from the negative terminal of the V_{EB} battery enters the base, which sets up a small base current I_B. Each hole entering the collector region combines with an electron from the negative terminal of the V_{CB} battery and gets neutralised and thus creates a collector current I_C. Here the emitter current I_E divides to give the base current I_B and the collector current I_C, such that

$$I_E = I_B + I_C$$

Thus, inside the *pnp* transistor, the current conduction is due to holes while electrons are the charge carriers in the external circuit.

ILLUSTRATION 24

In an npn transistor circuit, the collector current is 10 mA. If 95% of the electrons emitted reach the collector, what is the base current?

SOLUTION

Given that $I_C = 95\% I_E$

$$\Rightarrow \quad I_C = 0.95 I_E$$

$$\Rightarrow \quad I_E = \frac{I_C}{0.95} = \frac{100}{95} \times 10 \text{ mA}$$

$$\Rightarrow \quad I_E = 10.53 \text{ mA}$$

Since, $I_E = I_C + I_B$

So, the base current is given by

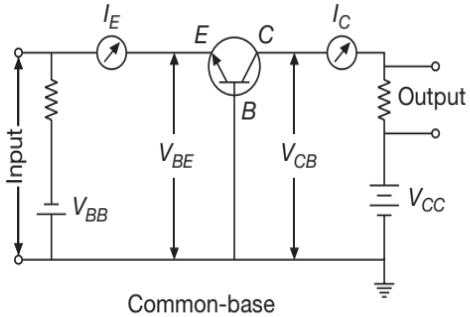
$$I_B = I_E - I_C = 10.53 - 10 = 0.53 \text{ mA}$$

THREE CONFIGURATIONS OF A TRANSISTOR

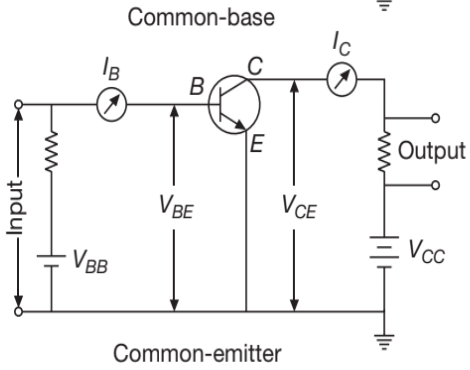
A transistor is a three element device. One terminal has to be always common to the input and the output circuits. This terminal is connected to the ground and serves as a reference point for the entire circuit. So, a transistor can be used in one of the following three configurations

(a) Common-base (CB) circuit.
(b) Common-emitter (CE) circuit.
(c) Common-collector (CC) circuit.

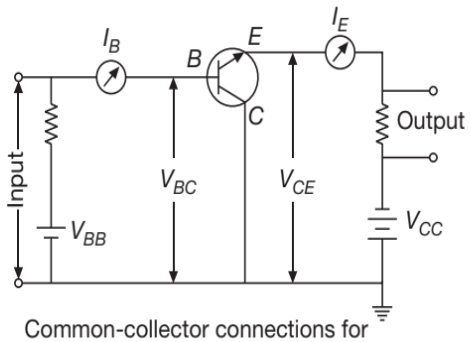
The three types of circuit arrangements for an *npn* transistor are shown in figure.



Common-base



Common-emitter



Common-collector connections for *npn* transistor

In each case, the emitter-base junction is forward biased whereas the collector-base junction is reverse biased.

CURRENT GAIN FOR A TRANSISTOR

We define two types of current gains for a transistor.

(a) Common base configuration current gain: This current gain is denoted by α. It is also called as common base current amplification factor or the ac current gain.
It is defined as the ratio of the small change in the collector current to the small change in the emitter current when the collector-base voltage is kept constant. Thus

$$\alpha = \left(\frac{\Delta I_C}{\Delta I_E}\right)_{V_{CB}=\text{constant}}$$

(b) Common emitter configuration current gain: This current gain is denoted by β. It is also called as common emitter current amplification factor or the ac current gain.
It is defined as the ratio of the small change in the collector current to the small change in the base current when the collector-emitter voltage is kept constant. Thus

$$\beta = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE}=\text{constant}}$$

RELATION BETWEEN α AND β

Since we know that, for both *npn* and *pnp* transistors

$$I_E = I_B + I_C$$

For small changes in the currents, we can re-write the above equation as

$$\Delta I_E = \Delta I_B + \Delta I_C$$

Dividing both sides by ΔI_C, we get

$$\frac{\Delta I_E}{\Delta I_C} = \frac{\Delta I_B}{\Delta I_C} + 1$$

Since, $\frac{\Delta I_C}{\Delta I_E} = \alpha$ and $\frac{\Delta I_C}{\Delta I_B} = \beta$, so we get

$$\frac{1}{\alpha} = \frac{1}{\beta} + 1$$

$$\Rightarrow \quad \alpha = \frac{\beta}{1+\beta} \text{ OR } \beta = \frac{\alpha}{1-\alpha}$$

As the value of I_B is about 1% to 5% of I_E or I_C is 95% to 99% of I_E, so α is about 0.95 to 0.99 and β is about 20 to 100. The CE configuration is frequently used because it gives high current gain as well as voltage gain.

Conceptual Note(s)

(a) It is observed that, if the emitter-base junction is forward biased and the collector-base junction is reverse biased, then too α and β are independent of current

(b) Please note that, the above definitions of α and β do not hold when both the junctions of a transistor are forward biased or reverse biased.

ILLUSTRATION 25

The current gain for common base amplifier is 0.98. Calculate the current amplification factor, if the transistor is being used in the common emitter configuration.

SOLUTION

If α is the current amplification factor for common base amplifier and β is the current amplification for common emitter amplifier, then it is given that $\alpha = 0.98$

Since, $\beta = \frac{\alpha}{1-\alpha}$

$$\Rightarrow \quad \beta = \frac{0.98}{(1-0.98)} = 49$$

ILLUSTRATION 26

The current factor of a transistor in a common base arrangement in 0.98. Calculate the change in collector current corresponding to a change of 5 mA in the emitter current. Also calculate the change in base current.

SOLUTION

Given that, $\alpha = 0.98$ and $\Delta I_E = 5.0$ mA

From the definition of $\alpha = \frac{\Delta I_C}{\Delta I_E}$

Change in collector current,

$$\Delta I_C = (\alpha)(\Delta I_E) = (0.98)(5) \text{ mA} = 4.9 \text{ mA}$$

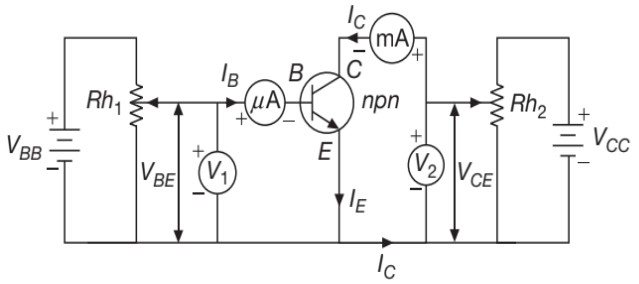
Further, change in base current,

$$\Delta I_B = \Delta I_E - \Delta I_C = 0.1 \text{ mA}$$

COMMON EMITTER TRANSISTOR CHARACTERISTICS

The common emitter characteristics are the graphs drawn between appropriate voltages and currents for a transistor when its emitter is taken as the common terminal and grounded (i.e. taken at zero potential), base is the input terminal and collector is the output terminal.

The circuit diagram for studying the common emitter characteristics of an *npn* transistor is shown in Figure.



Circuit for studying the common-emitter characteristics of an *npn* transistor

The emitter base junction is forward biased by means of the battery V_{BB} through a rheostat Rh_1. The emitter collector circuit is reverse biased by means of battery V_{CC} through a rheostat Rh_2.

The base emitter voltage V_{BE} and the collector emitter voltage V_{CE} are measured by using high resistance voltmeters.

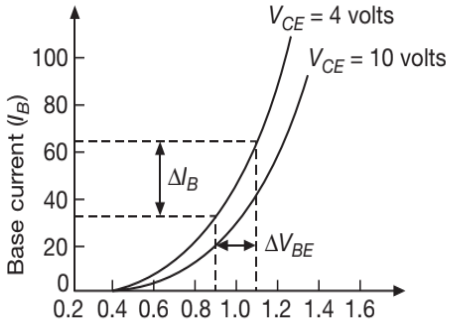
The base current I_B is measured by a microammeter and the collector current I_C by a milliammeter.

Three types of characteristic curves are studied.

(a) The input characteristic curve.
(b) The output characteristic curve.
(c) The transfer characteristic curve.

INPUT CHARACTERISTIC CURVE OF A TRANSISTOR

The input characteristic curve of a transistor is a graph showing the variation of base current I_B with base emitter voltage V_{BE} at constant collector emitter voltage V_{CE}. Curves for two different collector emitter voltages applied across *npn* transistor have been plotted in figure.



Input characteristics of *CE npn* transistor

A detailed study of these curves reveals the following facts.

(a) As long as V_{BE} is less than the barrier voltage, the base current I_B is small just similar to the case of a forward biased diode.
(b) As soon as the base emitter voltage V_{BE} exceeds the barrier voltage, the base current I_B increases sharply with a small increase in V_{BE} just like the case of a forward biased diode.
(c) The value of I_B is much smaller than that in a normal diode because more than 95% majority emitter carriers (electrons in *npn* and holes in *pnp* transistor) go to the collector to constitute the collector current I_C.

Since the increase in V_{CE} appears as the increase in V_{CB}, so its effect on I_B is negligible, due to which the input characteristic for various values of V_{CE} give almost identical curves. Hence, it is sufficient enough to determine only one input characteristic.

Input Resistance of a Transistor

The input resistance (r_i) of the transistor in CE configuration is defined as the ratio of the small change in base emitter voltage to the corresponding small change in the base current, when the collector emitter voltage is kept fixed. Mathematically,

$$r_i = \left(\frac{\Delta V_{BE}}{\Delta I_B}\right)_{V_{CE}=\text{constant}}$$

Since the input characteristic curve is non-linear, so r_i varies. However, at any point of the input characteristic curve, r_i is equal to the slope of the tangent drawn

at that point to the curve. *The input resistance can have a value ranging from few hundred to few thousand ohms.*

ILLUSTRATION 27

The current amplification factor for a common emitter arrangement is 59. If the emitter current is 5 mA. Calculate the value of collector current.

SOLUTION

Current amplification factor for common emitter amplifier is given to be $\beta = 59$ and the emitter current is $I_E = 5$ mA

Since, $\alpha = \dfrac{\beta}{1+\beta}$

Also $\alpha = \dfrac{I_C}{I_E}$

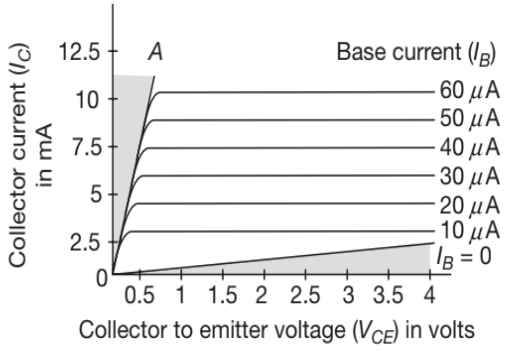
$$\Rightarrow \quad \frac{I_C}{I_E} = \frac{\beta}{1+\beta}$$

$$\Rightarrow \quad I_C = \left(\frac{\beta}{1+\beta}\right) I_E$$

$$\Rightarrow \quad I_C = \left(\frac{59}{60}\right) \times 5 = 4.92 \text{ mA}$$

OUTPUT CHARACTERISTIC CURVE OF A TRANSISTOR

The output characteristic curve of a transistor is a graph showing the variation of collector current I_C with collector emitter voltage V_{CE} at constant base-current I_B is called the output characteristic of the transistor. Curves for different values of I_B for *npn* transistor have been plotted in figure.



Output characteristic of *CE npn* transistor

A detailed study of these curves reveals the following facts.

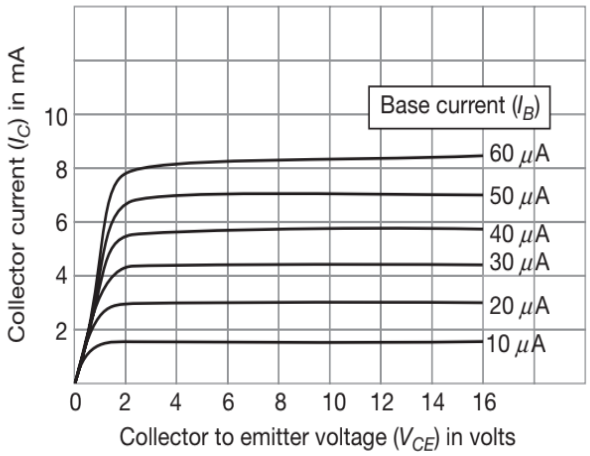
(a) When the voltage V_{CE} increases from zero volt to about 0.5 V, the collector current I_C increases rapidly. The value of V_{CE} upto which I_C increases rapidly is called Knee Voltage.

(b) Once the voltage V_{CE} exceeds the voltage V_{BE} (so that the collector base junction is reverse biased), the output current I_C varies very slowly but linearly with V_{CE} for a given base current I_B. This makes us conclude that beyond the knee voltage, the output resistance of the transistor is high.

(c) For a given V_{CE}, the larger the value of I_B, the larger is the value of I_C.

ILLUSTRATION 28

From the output characteristics of a common emitter transistor shown in figure, calculate the values of β_{ac} and β_{dc} of the transistor when V_{CE} is 10 V and $I_C = 4$ mA.



SOLUTION

Since, we know that

$$\beta_{ac} = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE}} \text{ and } \beta_{dc} = \frac{I_C}{I_B}$$

For calculating β_{ac} and β_{dc} at the asked values of V_{CE} and I_C, consider any two characteristics for two values of I_B which lie above and below the given value of I_C.

Given that $I_C = 4$ mA, so let us select two values of I_B i.e. $I_B = 30\ \mu$A and $I_B = 20\ \mu$A. At $V_{CE} = 10$ V

we read the two values of I_C from the graph, then we have

$$\Delta I_B = (30-20)\ \mu A = 10\ \mu A,$$

$$\Delta I_C = (4.5-3)\ mA = 1.5\ mA$$

$$\Rightarrow \quad \beta_{ac} = \frac{\Delta I_C}{\Delta I_B} = \frac{1.5\ mA}{10\ \mu A} = 150$$

For calculating β_{dc}, we can either estimate the value of I_B corresponding to $I_C = 4$ mA at $V_{CE} = 10$ V or we can calculate the two values of β_{dc} for the two characteristics chosen and then calculate their mean value

So, for $I_C = 4.5$ mA, $I_B = 30\ \mu A$, we have

$$\beta_1 = \frac{4.5\ mA}{30\ \mu A} = 150$$

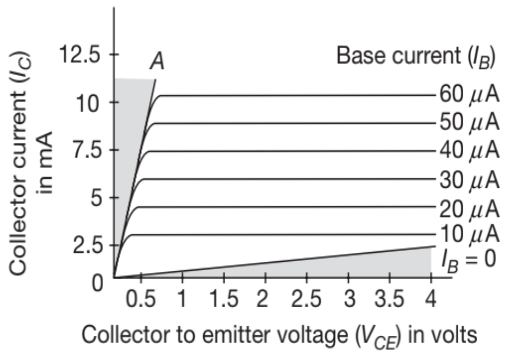
and for $I_C = 3$ mA, $I_B = 20\ \mu A$, we have

$$\beta_2 = \frac{3\ mA}{20\ \mu A} = 150$$

$$\Rightarrow \quad \beta_{dc} = \frac{\beta_1 + \beta_2}{2} = \frac{150+150}{2} = 150$$

Three Regions of the Output Characteristic Curve of a Transistor

We have shaded different regions in the output characteristic curve of an *npn* transistor for different values of I_B.



Output characteristic of *CE npn* transistor

(a) The shaded region towards the left of line OA is called saturation region and the line OA is called saturation line. Here $V_{CE} < V_{BE}$. Both the junctions are forward biased. Here I_C does not depend on the input current I_B.

(b) The shaded region lying below the curve for $I_B = 0$ is called cut-off region. In this region, both the junctions are reverse biased. Here $I_C = 0$. In the shaded regions, the transistor works as switch, it turns over rapidly from OFF state for which $I_C = 0$ (cut-off) to the ON state for which I_C is maximum (saturation state).

(c) The non-shaded central region of the output characteristic is called active region. In this region, the emitter-base junction is forward biased and the collector-base junction is reverse biased. A transistor works as an audio amplifier in this region.

Output Resistance of a Transistor

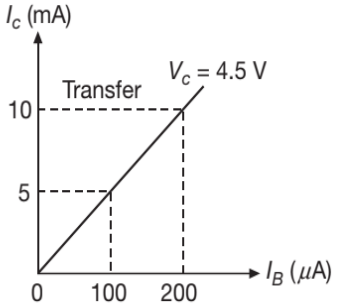
The output resistance r_o of a transistor in CE configuration is defined as the ratio of the small change in the collector-emitter voltage to the corresponding change in the collector current when the base current is kept constant. Thus

$$r_0 = \left(\frac{\Delta V_{CE}}{\Delta I_C}\right)_{I_B = \text{constant}}$$

The reciprocal of the slope of the linear part of the output characteristic curve (i.e. I_C vs V_{CE} curve) gives the value of output resistance. The output resistance of the transistor is mainly controlled by the bias of the base-collector junction. The output resistance is of the order of few hundred kilo ohms.

TRANSFER CHARACTERISTIC CURVE OF A TRANSISTOR

The transfer characteristic curve of a transistor is a graph showing the variation of collector current I_C with the base current I_B at constant collector emitter voltage V_{CE}. The transfer characteristic of a transistor is almost a straight line as shown in Figure.



Transfer characteristic of *CE npn* transistor

CURRENT AMPLIFICATION FACTOR (β)

It is defined as the ratio of the change in collector current to the small change in base current at constant collector-emitter voltage (V_{CE}) when the transistor is in the active state.

$$\beta_{ac} = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE}=\text{constant}}$$

This is also known as small signal current gain and its value is very large. The direct ratio of I_C and I_B gives the dc current gain (β_{dc}) of the transistor. Hence,

$$\beta_{dc} = \frac{I_C}{I_B}$$

Since I_C increases with I_B almost linearly and $I_C = 0$ when $I_B = 0$, the values of both β_{ac} and β_{dc} are nearly equal.

ADVANTAGES OF TRANSISTORS

Transistors, because of their many merits over vacuum tubes, have practically completely replaced them. Some of the advantages of the transistors over the vacuum tubes are as given below

Advantages

(a) Transistors require low voltages for their operation as compared to vacuum tubes.
(b) Since no heating is required, transistors are set into operation as soon as the circuit is switched on.
(c) Due to their small sizes, the circuits involving transistors are very compact.
(d) Transistors have almost unlimited life.
(e) Since transistors have no filaments, hence no power is needed to heat them to cause the emission of electrons.
(f) Since no vacuum has to be created in transistors, they have no vacuum deterioration trouble.
(g) Transistors are shock proof.
(h) During operation, transistors do not produce any humming noise.
(i) Transistors are cheaper as compared to vacuum tubes.

Transistors enjoy a number of advantages over the vacuum tubes still they have following drawbacks which put restrictions on their use in electronic circuits.

DRAWBACKS OF TRANSISTORS

(a) Ordinary semiconductor devices cannot handle as much power as ordinary vacuum tubes can do.
(b) The transistors are temperature-sensitive. The maximum temperature the transistors can withstand, is very low $(\approx 50\ ^\circ\text{C})$. Even a small overheating spoils the transistor. This is because, at a higher temperature, the covalent bonds break up and the semiconductor piece forming the transistor becomes conducting.
(c) Noise level is higher in transistors as compared to that in the vacuum tubes.
(d) They show poor response for high frequency range.

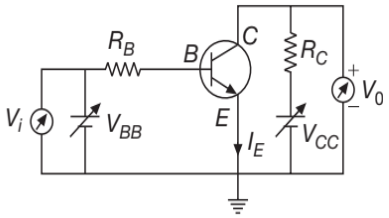
TRANSISTOR AS A SWITCH

Modern day digital devices like computers perform millions of switching operations per day. For such operations, transistors can be used as switches in computer circuits because they act swiftly. It has been observed that transistors have many advantages over other electrically operated switches such as relays and reed switches. This is because, the transistors

(a) are small, cheap and reliable.
(b) can switch on and off millions of times a second.
(c) have long life in well designed circuits.
(d) have no moving parts.

Three States of a Transistor

To understand the operation of a transistor as a switch, we first study the three states or conditions in which a transistor can work. Figure shows the circuit diagram of a base-biased *npn* transistor in CE configuration. Let R_B be the resistance in the input circuit and R_C be the resistance in the output circuit.



A base biased *npn* transistor in *CE* configuration

Applying Kirchhoff's rule to the input and output circuits separately, we get

$$V_{BB} - I_B R_B - V_{BE} = 0$$

$$\Rightarrow \quad V_{BB} = I_B R_B + V_{BE}$$

and $\quad V_{CC} - I_C R_C - V_{CE} = 0$

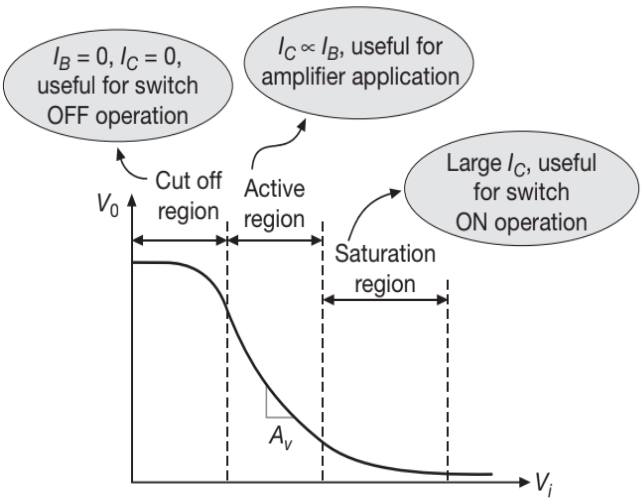
$$\Rightarrow \quad V_{CE} = V_{CC} - I_C R_C$$

The voltage V_{BB} can be regarded as the dc input voltage V_i and V_{CE} as the dc output voltage V_0. So, we can write

$$V_i = I_B R_B + V_{BE}$$

and $\quad V_0 = V_{CC} - I_C R_C \quad \ldots(1)$

Figure shows a typical output voltage (V_0) plotted against the input voltage (V_i) characteristic, called the transfer characteristic of the base biased transistor. As discussed already, it has three well-defined regions.



Transfer characteristic of base-biased transistor

Cut-off Region

When V_i increases from zero to a low value (less than 0.6 V in case of a Si transistor), the forward bias of the emitter-base junction is insufficient to start a forward current. That is, $I_B = 0$ and hence $I_C = 0$. The transistor is said to be in the *cutoff region*. From equation (1), the output voltage is given by $V_0 = V_{CC}$.

Active Region

When V_i increases slightly above 0.6 V, a current I_C flows in the output circuit and the transistor is said to be in the *active region*. Since we have

$$V_0 = V_{CC} - I_C R_C$$

So, as the term $I_C R_C$ increases, the output voltage V_0 decreases. Now as V_i increases, I_C increases almost linearly and so V_0 decreases linearly till its value becomes less than 1.0 V.

Saturation Region

When the input voltage V_i is high i.e., the emitter-base junction is heavily forward biased, then the collector current I_C is large, due to which it a large potential drop across load resistance R_C is produced such that the emitter-collector junction also gets forward biased. Hence the output voltage V_0 decreases to almost zero and the transistor is said to be in the *saturation state* because it cannot pass any more collector current I_C.

Conceptual Note(s)

Please note that, the transitions from cutoff state to active state and from active state to saturation state are not sharply defined because these regions of the transfer characteristic are non-linear.

Switching Action of a Transistor

A transistor can be used as a switch when it is operated in cutoff and saturation states only. The design of a switch circuit is such that the transistor does not remain in the active state.

As long as the input voltage is low and unable to forward-bias the transistor, the output voltage V_0 (at V_{CC}) is high. When V_i is high enough to drive the transistor into saturation, then V_0 is low, nearly zero. When the transistor is not conducting, it is said to be switched off and when it is driven into saturation, it is said to be switched on. Corresponding to cutoff and saturation voltages of the transistor, if we define the low (0) and the high (1) states as below and above certain voltage levels, then a low input switches the transistor off and a high input switches it on. Alternatively, we can say that a low input to the transistor gives a high output and high input gives a low output.

AMPLIFYING ACTION OF A TRANSISTOR

For considering the transistor as an amplifier we will use the transistor in the Active mode as shown earlier in the output voltage (V_0) plotted against the input voltage (V_i) graph. When the base-emitter junction of a transistor is forward biased, the depletion layer about this junction is much smaller than the depletion layer around the base-collector junction which is reverse biased. Thus, the resistance R_{EB} of the emitter-base junction is much smaller than the resistance R_{BC} of the collector-base junction. So, power dissipation in the emitter base circuit is given by

$$P_{EB} = I_E^2 R_{EB}$$

Similarly, power dissipation in the base collector circuit is

$$P_{BC} = I_C^2 R_{BC}$$

Since, $I_E \approx I_C$ and $R_{BC} \gg R_{EB}$

$$\Rightarrow \quad P_{BC} \gg P_{EB}$$

i.e., the power dissipated in the base-collector circuit is much higher than the power dissipated in the emitter-base circuit or output power is much greater than the input power. This phenomenon is called *the amplifying action of a transistor*.

The base region of a transistor is very thin and lightly doped. A thin and lightly doped base region contains a smaller number of majority charge carriers. This reduces the rate of recombination of electrons and holes at the emitter-base junction. Most $(95-99\%)$ of the majority charge carriers, diffusing from emitter to base, reach the collector. Thus, the base current is small and the collector is almost equal to the emitter current. This results in the large voltage gain and power gain of the transistor.

Conceptual Note(s)

TRANSISTOR: A WORD MADE FROM TRANSFER AND RESISTOR

The resistance offered by the emitter-base junction to the flow of current is small because it is forward biased. Similarly, the resistance offered by the base-collector junction to the flow of current is large because this junction is reverse biased. However, since the collector current I_C is almost equal to the emitter current I_E, so we can say that the current is transferred from the low resistance circuit to the high resistance circuit. Hence the name transistor, which is combination of the words transfer and resistor.

TRANSCONDUCTANCE

For the case of a voltage amplifier, the input signal to be amplified is superposed on a steady voltage V_{EB} applied across the emitter-base junction. For a high voltage gain (the ratio of output voltage to the input voltage), the change in the collector current (ΔI_c) should be as large as possible, for a given change in the emitter-base voltage (ΔV_{EB}). So, we can define a new term that acts as a figure of merit for a transistor and this term is called the Transconductance.

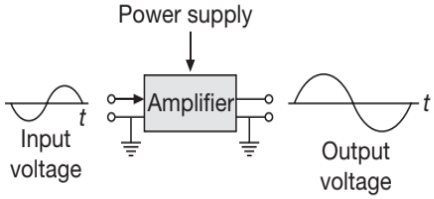
Transconductance is defined as the ratio of the small change in the collector current to the small change in the emitter-base voltage. It is denoted by g_m. Thus

$$g_m = \frac{\Delta I_C}{\Delta V_{BE}}$$

The transconductance is also called transfer conductance and has the same units of conductance (i.e. siemen or mho). The transconductance depends on the geometry, doping levels and biasing of the transistor.

CONCEPT OF AN AMPLIFIER

An **amplifier** is a circuit which consists of at least one transistor that can be used for increasing the voltage, current or power of ac input. To amplify means to increase the size or to magnify an input signal. The output signal of an amplifier is an enlarged version of the input signal. The general concept of an amplifier or simply the block diagram of the amplifier is shown in the Figure.



The concept of an amplifier

The amplifier has

(a) two input terminals across which the signal to be amplified is fed.
(b) two output terminals for connecting the load across which the amplified output is to be taken and
(c) a power supplying assembly to supply power to the amplifier.
(d) one input terminal and one output terminal (which is common to the input and output) earthed.

AC VOLTAGE GAIN (A_V)

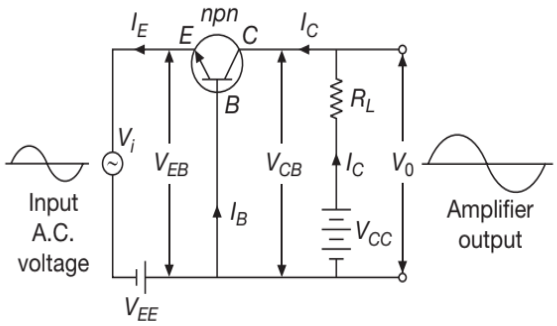
The usefulness of an amplifier is expressed in terms of the gain of the amplifier. The ac voltage gain of an amplifier is defined as the ratio of the change in the output voltage (ΔV_0) to the corresponding change in the input voltage (ΔV_i). Thus

$$A_V = \frac{\Delta V_0}{\Delta V_i}$$

The voltage gain of an amplifier is always greater than unity. Please note that, only the ac and not the dc components of the input and the output voltages are used to calculate the voltage gain.

NPN TRANSISTOR AS COMMON BASE AMPLIFIER

For an *npn* transistor used as a common base amplifier, the base is common to both input and output circuits. The emitter base junction is forward biased by the battery V_{EE} and the collector base junction is reverse biased by battery V_{CC} as shown in the Figure.



npn transistor as a common base amplifier

Due to this biasing technique, the resistance R_{in} of input circuit decreases and the resistance R_{out} of output circuit increases i.e. $R_{out} > R_{in}$. A low input ac signal is superimposed on the forward bias V_{EB} of the emitter base junction and a load resistance R_L is connected between the collector and dc supply. The amplified output is obtained between collector and ground. When no ac signal is fed to the input circuit, then

$$I_E = I_B + I_C$$

When a current I_C flows in the output circuit, a voltage drop $I_C R_L$ occurs across the load R_L. The output voltage V_0 is calculated by applying Kirchhoff's Loop Law (KLL) and is given by

$$V_0 = V_{CB} = V_{CC} - I_C R_L \qquad \ldots(1)$$

When the input signal V_i is applied across the emitter-base circuit, then it changes the emitter-base voltage and hence the emitter current I_E is also changed. Due to change in the emitter current I_E, the collector current I_C also changes and hence the output voltage V_0 also changes in accordance with equation (1). This variation in the collector voltage appears as amplified output.

Phase Between Input and Output Signals

When ac signal is fed to the input circuit, then its positive half cycle decreases the forward bias. This decreases the emitter current and the collector current, due to which the potential drop $(I_C R_L)$ across load resistance decreases and hence V_0 increases. Since collector is connected to the positive terminal of the V_{CC} battery, so increase in V_0 implies that it becomes more positive and hence an amplified half output is obtained. So, as the input signals goes through its positive half cycle, the output signal also goes through a positive half cycle.

Similarly, as the input signal goes through its negative half cycle, the output signal also goes through its negative half cycle. Hence in a common base amplifier, the input and output voltages are in same phase.

CURRENT, VOLTAGE AND POWER GAIN FOR A COMMON BASE AMPLIFIER

AC Current Gain (α)

It is defined as the ratio of the small change in the collector current (ΔI_C) to the small change in the emitter current (ΔI_E) at constant collector-base voltage. It is commonly denoted by α_{ac} or sometimes is also denoted by A_i. So

$$\alpha_{ac} = A_i = \left(\frac{\Delta I_C}{\Delta I_E}\right)_{V_{CB}=\text{constant}}$$

DC Current Gain (α_{dc})

It is defined as the ratio of the collector current to the emitter current, at constant collector-base voltage. Mathematically,

$$\alpha_{dc} = \left(\frac{I_C}{I_E}\right)_{V_{CB}=\text{constant}}$$

AC Voltage Gain (A_V)

It is defined as the ratio of the small change in output voltage (ΔV_{CB}) to the small change in input voltage ΔV_{EB}. So,

$$A_V = \frac{\Delta V_{CB}}{\Delta V_{EB}}$$

Since, $\Delta V_{CB} = (\Delta I_C) R_0$ and $\Delta V_{EB} = (\Delta I_E) R_i$

where R_i is the resistance of input circuit and R_0 is the resistance of output circuit (including R_L).

$$\Rightarrow \quad A_V = \left(\frac{\Delta I_C}{\Delta I_E}\right)\left(\frac{R_0}{R_i}\right) = \alpha_{ac}\left(\frac{R_0}{R_i}\right)$$

$$\Rightarrow \quad A_V = A_i \times A_r$$

$$\Rightarrow \quad \begin{pmatrix}\text{Voltage}\\ \text{Gain}\end{pmatrix} = \begin{pmatrix}\text{Current}\\ \text{Gain}\end{pmatrix} \times \begin{pmatrix}\text{Resistance}\\ \text{Gain}\end{pmatrix}$$

AC Power Gain (A_P)

It is defined as the ratio of the small change in output power to the small change in input power.

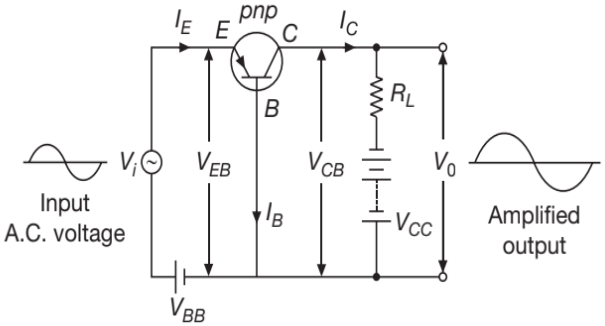
$$A_P = \frac{\text{Change in output power}}{\text{Change in input power}}$$

$$\Rightarrow \quad A_P = \frac{(\Delta I_C)^2 R_0}{(\Delta I_E)^2 R_i} = \left(\frac{\Delta I_C}{\Delta I_E}\right)^2 \left(\frac{R_0}{R_i}\right)$$

$$\Rightarrow \quad A_P = \alpha_{ac}^2 \left(\frac{R_0}{R_i}\right) = \alpha_{ac}^2 \,(\text{Resistance Gain})$$

PNP TRANSISTOR AS COMMON BASE AMPLIFIER

For a *pnp* transistor used as a common base amplifier, the base is common to both input and output circuits. The emitter base junction is forward biased by the battery V_{EE} and the collector base junction is reverse biased by battery V_{CC} as shown in the figure.



pnp transistor as a common base amplifier

Due to this biasing technique, the resistance R_{in} of input circuit decreases and the resistance R_{out} of output circuit increases i.e. $R_{out} > R_{in}$. A low input ac signal V_i is superimposed on the forward bias V_{EB} of the emitter base junction and a load resistance R_L is connected between the collector and dc supply. The amplified output is obtained between collector and ground. When no ac signal is fed to the input circuit, then

$$I_E = I_B + I_C$$

When a current I_C flows in the output circuit, a voltage drop $I_C R_L$ occurs across the load R_L. The output voltage V_0 is calculated by applying Kirchhoff's Loop Law (KLL) and is given by

$$V_0 = V_{CB} = V_{CC} - I_C R_L \qquad \ldots(1)$$

When the input signal V_i is applied across the emitter-base circuit, then it changes the emitter-base voltage and hence the emitter current I_E is also changed. Due to change in the emitter current I_E, the collector current I_C also changes and hence the

output voltage V_0 also changes in accordance with equation (1). This variation in the collector voltage appears as amplified output.

Phase Between Input and Output Signals

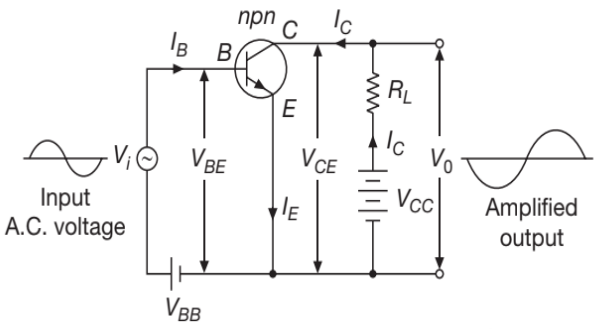
When ac signal is fed to the input circuit, then its positive half cycle increases the forward bias. This increases the emitter current and the collector current, due to which the potential drop $(I_C R_L)$ across load resistance increases and hence V_0 decreases. Since collector is connected to the negative terminal of the V_{CC} battery, so decrease in V_0 implies that it becomes less negative and hence more positive. Hence, an amplified half output is obtained, thus making us conclude that as the input signals goes through its positive half cycle, the output signal also goes through a positive half cycle.

Conceptual Note(s)

In a common base amplifier, the input and output voltages are in same phase i.e. phase angle between the input and the output voltage is 0°.

NPN TRANSISTOR AS COMMON EMITTER AMPLIFIER

For an *npn* transistor used as a common emitter amplifier, the emitter is common to both input and output circuits. The base emitter junction is forward biased by the battery V_{BB} and the collector emitter junction is reverse biased by battery V_{CC} as shown in the figure.



npn transistor as a common emitter amplifier

Due to this biasing technique, the resistance R_{in} of input circuit decreases and the resistance R_{out} of output circuit increases i.e. $R_{out} > R_{in}$. A low input ac signal V_i is superimposed on the forward bias V_{BE} of the base emitter junction and a load resistance R_L is connected between the collector and dc supply. The amplified output is obtained between collector and ground. When no ac signal is fed to the input circuit, then

$$I_E = I_B + I_C$$

When a current I_C flows in the output circuit, a voltage drop $I_C R_L$ occurs across the load R_L. The output voltage V_0 is calculated by applying Kirchhoff's Loop Law (KLL) and is given by

$$V_0 = V_{CE} = V_{CC} - I_C R_L \quad \ldots(1)$$

When the input signal V_i is applied across the base emitter circuit, then it changes the base emitter voltage and hence the emitter current I_E is also changed. Due to change in the emitter current I_E, the collector current I_C also changes and hence the output voltage V_0 also changes in accordance with equation (1). This variation in the collector voltage appears as amplified output.

Phase Between Input and output Signals

When ac signal is fed to the input circuit, then its positive half cycle increases the forward bias. This increases the emitter current and the collector current, due to which the potential drop $(I_C R_L)$ across load resistance increases and hence V_0 decreases. Since collector is connected to the positive terminal of the V_{CC} battery, so decrease in V_0 implies that it becomes less positive and hence more negative. Hence, an amplified half output is obtained, thus making us conclude that as the input signals goes through its positive half cycle, the output signal goes through a negative half cycle.

Similarly, as the input signal goes through its negative half cycle, the amplified output signal goes through its positive half cycle. Hence in a common emitter amplifier, the input and output voltages are 180° out of phase.

CURRENT, VOLTAGE AND POWER GAIN FOR A COMMON EMITTER AMPLIFIER

AC Current Gain (β)

It is defined as the ratio of the small change in the collector current (ΔI_C) to the small change in the base current (ΔI_B) at constant collector-emitter voltage. It is commonly denoted by β_{ac} or sometimes is also denoted by A_i. So

$$\beta_{ac} = A_i = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE}=\text{constant}}$$

DC Current Gain (β_{dc})

It is defined as the ratio of collector current to the base current, at constant collector-emitter voltage. Mathematically,

$$\beta_{dc} = \left(\frac{I_C}{I_B}\right)_{V_{CE}=\text{constant}}$$

In the linear region of the output characteristics, β_{ac} is usually close to β_{dc}.

AC Voltage Gain (A_V)

It is defined as the ratio of small change in output voltage ΔV_{CE} to the small change in input voltage ΔV_{BE}. So,

$$A_V = \frac{\Delta V_{CE}}{\Delta V_{BE}}$$

Since, $\Delta V_{BE} = R_i(\Delta I_B)$ and $\Delta V_{CE} = -R_0(\Delta I_C)$

where R_i is the resistance of the input or the emitter base circuit and R_0 is the resistance of the output or collector-emitter circuit (including R_L).

The negative sign indicates that the input and output voltages have a phase difference of 180° i.e., if the input voltage increases, the output voltage decreases.

$$\Rightarrow \quad A_V = -\left(\frac{\Delta I_C}{\Delta I_B}\right)\left(\frac{R_{\text{out}}}{R_{\text{in}}}\right) = -\beta_{ac}\left(\frac{R_{\text{out}}}{R_{\text{in}}}\right)$$

$$\Rightarrow \quad A_V = A_i \times A_r$$

$$\Rightarrow \quad \begin{pmatrix}\text{Voltage}\\ \text{Gain}\end{pmatrix} = \begin{pmatrix}\text{Current}\\ \text{Gain}\end{pmatrix} \times \begin{pmatrix}\text{Resistance}\\ \text{Gain}\end{pmatrix}$$

AC Power Gain (A_P)

It is defined as the ratio of the small change in output power to the small change in input power.

$$A_P = \frac{\text{Change in output power}}{\text{Change in input power}}$$

$$\Rightarrow \quad A_P = \frac{(\Delta I_C)^2 R_0}{(\Delta I_B)^2 R_i} = \left(\frac{\Delta I_C}{\Delta I_B}\right)^2\left(\frac{R_0}{R_i}\right)$$

$$\Rightarrow \quad A_P = \beta_{ac}^2\left(\frac{R_0}{R_i}\right) = \beta_{ac}^2\,(\text{Resistance Gain})$$

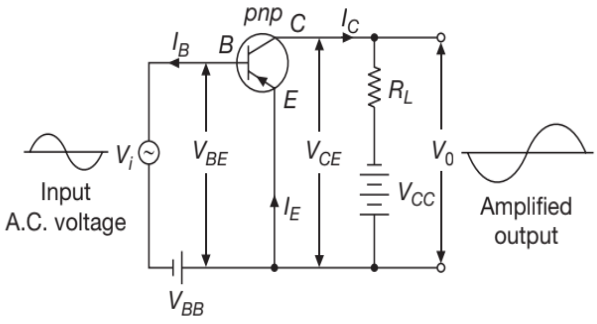
Since $\beta_{ac}^2 \gg \alpha_{ac}^2$, so the ac power gain of a common emitter amplifier is much larger than that of a common base amplifier.

Conceptual Note(s)

It may be noted that the transistor is not generating any power. The energy for the higher ac power at the output is supplied by the dc battery.

PNP TRANSISTOR AS COMMON EMITTER AMPLIFIER

For a *pnP* transistor used as a common emitter amplifier, the emitter is common to both input and output circuits. The base emitter junction is forward biased by the battery V_{BB} and the collector emitter junction is reverse biased by battery V_{CC} as shown in the figure.



pnp transistor as a common emitter amplifier

Due to this biasing technique, the resistance R_{in} of input circuit decreases and the resistance R_{out} of output circuit increases i.e. $R_{\text{out}} > R_{\text{in}}$. A low input ac signal V_i is superimposed on the forward bias V_{BE}

of the base emitter junction and a load resistance R_L is connected between the collector and dc supply. The amplified output is obtained between collector and ground. When no ac signal is fed to the input circuit, then

$$I_E = I_B + I_C$$

When a current I_C flows in the output circuit, a voltage drop $I_C R_L$ occurs across the load R_L. The output voltage V_0 is calculated by applying Kirchhoff's Loop Law (KLL) and is given by

$$V_0 = V_{CE} = V_{CC} - I_C R_L \quad \ldots(1)$$

When the input signal V_i is applied across the base emitter circuit, then it changes the base emitter voltage and hence the emitter current I_E is also changed. Due to change in the emitter current I_E, the collector current I_C also changes and hence the output voltage V_0 also changes in accordance with equation (1). This variation in the collector voltage appears as amplified output.

Phase Between Input and Output Signals

When ac signal is fed to the input circuit, then its positive half cycle decreases the forward bias. This decreases the emitter current and hence the collector current, due to which the potential drop $(I_C R_L)$ across load resistance decreases and hence the output voltage V_0 increases. Since collector is connected to the negative terminal of the V_{CC} battery, so increase in V_0 implies that it becomes more negative. Hence, an amplified half output is obtained, thus making us conclude that as the input signals goes through its positive half cycle, the output signal goes through a negative half cycle.

Similarly, as the input signal goes through its negative half cycle, the amplified output signal goes through its positive half cycle. Hence in a common emitter amplifier, the input and output voltages are $180°$ out of phase.

ILLUSTRATION 29

For a transistor connected in common emitter mode, if $R_0 = 4\ \text{k}\Omega$, $R_i = 1\ \text{k}\Omega$, $I_C = 1\ \text{mA}$ and $I_B = 20\ \mu\text{A}$, then calculate the voltage gain.

SOLUTION

The current gain for a transistor in common emitter mode is given by

$$\beta = \frac{I_C}{I_B} = \frac{1\times10^{-3}}{20\times10^{-6}} = 50$$

and the voltage gain in common emitter mode is

$$A_V = \beta\left(\frac{R_0}{R_i}\right) = (50)\left(\frac{4}{1}\right) = 200$$

ILLUSTRATION 30

A transistor is connected in common emitter configuration. The collector supply is $8\ \text{V}$ and voltage drop across a resistor of $800\ \Omega$ in the collector circuit is $0.5\ \text{V}$. If the current gain factor α is 0.96, calculate the base current.

SOLUTION

Given that, $V_{CC} = 8\ \text{V}$, $V_0 = I_C R_L = 0.5\ \text{V}$, $R_L = 800\ \Omega$ and $\alpha = 0.96$

Since, $\beta = \dfrac{\alpha}{1-\alpha}$

$$\Rightarrow \quad \beta = \frac{0.96}{1-0.96} = 24$$

Since, $V_0 = I_C R_L$

$$\Rightarrow \quad 0.5 = I_C \times 800$$

$$\Rightarrow \quad I_C = \frac{0.5}{800}\ \text{A}$$

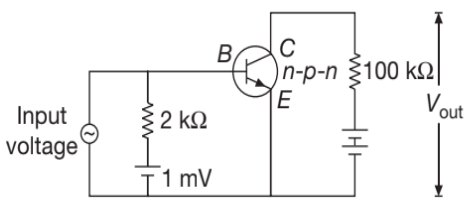
Since the current gain is given by $\beta = \dfrac{I_C}{I_B}$

$$\Rightarrow \quad I_B = \frac{I_C}{\beta} = \frac{\frac{0.5}{800}}{24} = 26\times10^{-6}\ \text{A}$$

$$\Rightarrow \quad I_B = 26\ \mu\text{A}$$

ILLUSTRATION 31

In the following common emitter configuration an npn transistor with current gain $\beta = 95$ is used. Calculate the output voltage of the amplifier.



SOLUTION

The input current i.e. the base current is given by

$$I_{in} = I_B = \frac{V_{in}}{R_{in}} = \frac{1\text{ mV}}{2\text{ k}\Omega}$$

$$\Rightarrow \quad I_B = 0.5\times10^{-6}\text{ A}$$

Since $\beta = \frac{I_{out}}{I_{in}} = \frac{I_C}{I_B}$

$$\Rightarrow \quad I_C = I_{out} = \beta I_B$$

$$\Rightarrow \quad I_C = 95\times0.5\times10^{-6}\text{ A}$$

$$\Rightarrow \quad I_C = 0.47\times10^{-4}\text{ A}$$

So, the output voltage is

$$V_0 = I_C R_L\text{, where } R_L = 100\text{ k}\Omega$$

$$\Rightarrow \quad V_0 = (0.47\times10^{-4}\text{ A})(100\text{ k}\Omega)$$

$$\Rightarrow \quad V_0 = 4.7\text{ mV}$$

ILLUSTRATION 32

A load of $3\text{ k}\Omega$ is connected in the collector branch of an amplifier circuit using a transistor in common emitter mode. The current gain is 40. The input resistance of the transistor is $0.40\text{ k}\Omega$. When the input current is changed by $40\ \mu\text{A}$, then calculate the change in output voltage, the change in the input voltage and the power gain.

SOLUTION

Given that

Load resistance $R_L = 3\text{ k}\Omega = 3\times10^3\ \Omega$,

Current gain $\beta = 40$

Input reistance $r_i = 0.40\text{ k}\Omega = 0.4\times10^3\ \Omega$ and

Change in base current $\Delta I_B = 40\ \mu\text{A} = 40\times10^{-6}\text{ A}$

So, output voltage V_0 is

$$V_0 = \Delta I_C R_L = \beta \Delta I_B R_L$$

$$\Rightarrow \quad V_0 = 40\times40\times10^{-6}\times3\times10^3 = 4.8\text{ V}$$

$$\Rightarrow \quad \Delta V_{BE} = \Delta I_B r_i = 40\times10^{-6}\times0.4\times10^3$$

$$\Rightarrow \quad \Delta V_{BE} = 16\times10^{-3}\text{ V}$$

and power gain is

$$A_P = \frac{\beta^2 R_L}{r_i}$$

$$\Rightarrow \quad A_P = (40)^2\left(\frac{3\times10^3}{0.4\times10^3}\right) = 12000$$

ILLUSTRATION 33

An *npn* transistor is connected in common emitter configuration in which collector supply is 8 V and the voltage drop across the load resistance of $800\ \Omega$ connected in the collector circuit is 0.8 V. If current amplification factor is 25, determine collector emitter voltage and base current. If the internal resistance of the transistor is $200\ \Omega$, calculate the voltage gain and the power gain.

SOLUTION

Voltage across the load resistance R_L is

$$V_0 = I_C R_L = 0.8\text{ V}$$

$$\Rightarrow \quad I_C = \frac{0.8}{R_L} = \frac{0.8}{800}\text{ A} = 1\text{ mA}$$

Since, $\beta = 25 = \frac{I_C}{I_B}$

$$\Rightarrow \quad I_B = \frac{I_C}{25} = 40\ \mu\text{A}$$

Since, $V_{CE} = V_{CC} - I_C R_L$

$$\Rightarrow \quad V_{CE} = (8-0.8)\text{ V} = 7.2\text{ V}$$

Voltage gain is

$$A_V = \beta\left(\frac{R_{out}}{R_{in}}\right)$$

$$\Rightarrow \quad A_V = 25\left(\frac{800}{200}\right) = 100$$

Power gain is

$$A_P = \beta^2\left(\frac{R_{out}}{R_{in}}\right) = (25)^2\left(\frac{800}{200}\right) = 2500$$

ILLUSTRATION 34

A pnp transistor is used in common emitter mode in an amplifier circuit. A change of $45\ \mu\text{A}$ in the base current brings a change of 3 mA in collector current

and 0.05 V in base emitter voltage. Calculate the input resistance r_i and the base current amplification factor (β). If a load of 7 kΩ is used, then calculatealso find the voltage gain of the amplifier.

SOLUTION

Given that, $\Delta I_B = 45\ \mu A = 45\times10^{-6}$ A,

$$\Delta I_C = 3\text{ mA} = 3\times10^{-3}\text{ A}$$

$$\Delta V_{BE} = 0.05\text{ V},\ R_L = 7\text{ k}\Omega = 7\times10^{3}\ \Omega$$

Input resistance

$$r_i = \frac{\Delta V_{BE}}{\Delta I_B} = \frac{0.05}{45\times10^{-6}} = 1.1\times10^{3}\ \Omega$$

Base current amplification factor

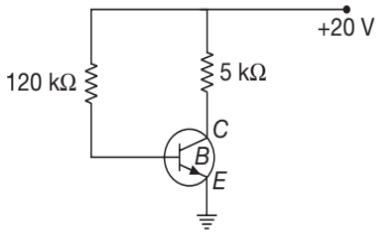
$$\beta = \frac{\Delta I_C}{\Delta I_B} = \frac{3\times10^{-3}}{45\times10^{-6}} = 66.67$$

Voltage gain of the amplifier

$$A_V = \beta\frac{R_L}{r_i} = \frac{66.67\times7\times10^{3}}{1.1\times10^{3}} = 424.27$$

ILLUSTRATION 35

In the following circuit, the value of β is 200. Find I_B, V_{CE}, V_{BE} and V_{BC}, when $I_C = 2.5$ mA. Find whether transistor is in active, cut off or saturation state.



SOLUTION

Since, $\beta = \dfrac{I_C}{I_B}$

$$\Rightarrow\quad I_B = \frac{I_C}{\beta} = \frac{2.5}{200} = 0.0125\text{ mA}$$

Applying Kirchhoff's Lop Law to base emitter loop, we get

$$V_{CE} = V_C - I_C R_C$$

$$\Rightarrow\quad V_{CE} = 20 - (2.5\times10^{-3})\times(5\times10^{3})$$

$$\Rightarrow\quad V_{CE} = 7.5\text{ V}$$

Similarly, we know that

$$V_{BE} = V_C - I_B R_B$$

$$\Rightarrow\quad V_{BE} = 20 - (0.0125\times10^{-3})\times(120\times10^{3})$$

$$\Rightarrow\quad V_{BE} = 18.5\text{ V}$$

$$\Rightarrow\quad V_{BC} = V_{BE} - V_{CE}$$

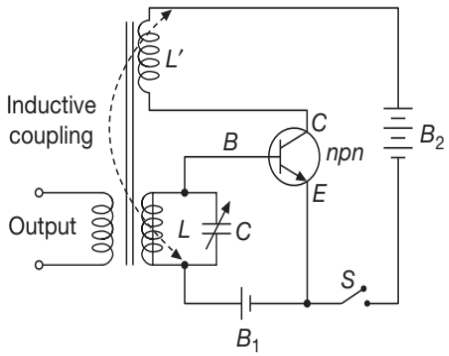
$$\Rightarrow\quad V_{BC} = (18.5 - 7.5)\text{ V} = 11\text{ V}$$

The transistor is in active state because base emitter junction is forward biased and the base collector junction is reverse biased.

TRANSISTOR AS AN OSCILLATOR

Oscillator is an electronic device that produces electric oscillations of constant frequency and amplitude, without the need of any external input signal. It converts dc energy obtained from a battery into ac energy in an oscillatory circuit.

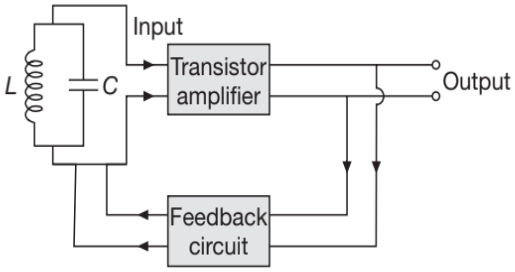
A basic circuit using a common-emitter *npn* transistor as an oscillator is shown in Figure.



A tank circuit consisting of an inductance L and a variable capacitor C is connected in the input or the emitter-base circuit which is forward biased. A small coil L' called feedback coil or tickler coil is connected in the output or the emitter-collector circuit which is reverse biased. The coil L' is inductively coupled with the coil L of the tank circuit.

Principle of an Oscillator

An oscillator may be regarded as the self-sustained transistor amplifier with a positive feedback. The block diagram of an oscillator is shown in Figure.



Principle for an oscillator

Essential Parts of an Oscillator

A transistor oscillator has the following essential parts.

(a) Tank circuit: A tank circuit is just a parallel combination of an inductance L and a capacitance C. The electric energy once given to it alternately changes between electrostatic energy in the capacitor and the magnetic energy in the inductor. The frequency of electric oscillations in the tank circuit is

$$f = \frac{1}{2\pi\sqrt{LC}}$$

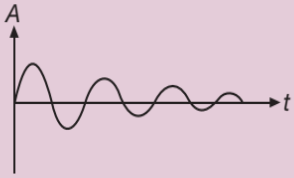
However, actually the oscillations get damped due to resistive losses in the inductance, and dielectric losses in the capacitor.

(b) Transistor amplifier: The oscillations of the tank circuit are fed to the transistor amplifier. The oscillations get amplified due to the amplifying action of the transistor.

(c) Feedback circuit: To compensate for the energy losses occurring in the tank circuit, the feedback circuit returns (feeds back) a part of the output power of the transistor amplifier to the tank circuit in phase with the input signal. *This process is called positive feedback* and produces undamped oscillations. The feedback may be done through inductive coupling (mutual inductance).

Conceptual Note(s)

Need for positive feedback: The oscillations are damped due to the presence of some inherent electrical resistance in the circuit. Consequently, the amplitude of oscillations decreases rapidly and the oscillations ultimately stop. Such oscillations are of little practical importance. In order to obtain oscillations of constant amplitude, we make an arrangement for **regenerative** or **positive feedback** from the output circuit to the input circuit so that the losses in the circuit can be compensated.



WORKING OF AN OSCILLATOR

When the switch S is closed, a small collector current starts growing through coil L'. This increases the magnetic flux linked with coil L' and hence with coil L (because both are inductively coupled). This induces an emf in the coil L that supports the forward bias and a positive charge begins to build on the upper plate of capacitor C. Due to this, the emitter current increases and hence the collector current also increases. This increases the magnetic flux linked with L' and hence with L. Consequently, the forward bias increases due to which the emitter current and the collector current also increase. Because of this, the charging of the capacitor continues and this process continues till the collector current becomes maximum.

Now, when the current through L' stops changing, the induced emf linked with L vanishes. This decreases the emitter current and hence the collector current. The decreasing current through L' induces an emf in L that opposes the forward bias, which results in decrease in the emitter current and hence the collector current. At the same instant, the positive charge on the lower plate of capacitor C begins to build up. The process continues till the collector current becomes zero, but the inertia of the collapsing magnetic field carries the collector current below the zero value. The induced emf linked with L again becomes zero, i.e. the forward bias is now not being opposed by induced emf. The emitter current and hence the collector current will start increasing. This cycle repeats again and again to give electric oscillations of constant amplitude and of constant frequency,

$$f = \frac{1}{2\pi\sqrt{LC}}$$

The oscillations of a desired frequency can be obtained by changing the value of capacitance C of the variable capacitor.

Conceptual Note(s)

(a) If the tank circuit is connected on the base side (as done above), then the oscillator is called as a tuned base oscillator.

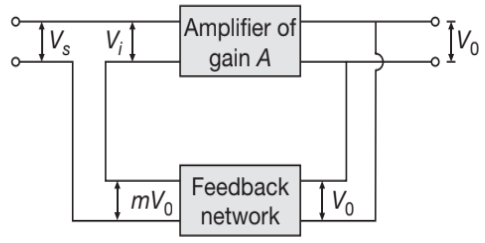
(b) If the tank circuit is connected on the collector side, then the oscillator is also called as a tuned collector oscillator.

(c) In the common emitter transistor circuit, a signal applied to the base emitter circuit appears with a phase change of 180° in the collector emitter circuit. The coupling of L and L' produces a further phase change of 180° due to mutual induction. Hence the energy fed back to the tank circuit is in phase with the input signal. Due to this positive feedback, the oscillations of the tank circuit are correctly maintained.

BARKHAUSEN'S CRITERION FOR SUSTAINED OSCILLATIONS

When a part of the output is fed back to the input of an amplifier, the process is called feedback process. Figure shows a feedback amplifier with input V_S and output V_0. The voltage gain of the feedback amplifier is

$$A'_V = \frac{\text{Output}}{\text{Input}} = \frac{V_0}{V_s}$$



Principle of feedback oscillator.

The input given to the feedback network is V_0. If m is the feedback fraction of the feedback network, then output obtained from it is mV_0. This fraction is mixed with the signal voltage V_s and is given to the amplifier.

$\Rightarrow$ Input of the amplifier, $V_i = V_s + mV_0$

The voltage gain of the amplifier is

$$A = \frac{\text{Output}}{\text{Input}} = \frac{V_0}{V_s + mV_0}$$

$$\Rightarrow \quad AV_s + AmV_0 = V_0$$

$$\Rightarrow \quad AV_s = V_0(1 - mA)$$

$$\Rightarrow \quad \frac{V_0}{V_s} = \frac{A}{1 - mA}$$

Hence the voltage gain of the feedback amplifier is

$$A'_V = \frac{V_0}{V_s} = \frac{A}{1 - mA}$$

When $mA = 1$, $A'_V = \frac{V_0}{V_s} \to \infty$. This means $V_s = 0$

Thus, the output voltage is obtained without the input voltage. The amplifier becomes a self-sustained oscillator. Hence the condition for stable oscillations to be sustained is $mA = 1$. *This is known as Barkhausen's criterion for sustained oscillations.*

Conceptual Note(s)

If the feedback is negative, the gain of the amplifier becomes

$$A'_V = \frac{A}{1 + mA}$$

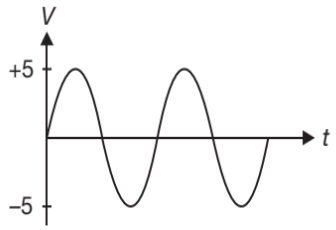
In an oscillator, the feedback is in same phase (positive feedback). If the feedback voltage is in opposite phase (negative feedback), the gain is less than 1 and it can never work as an oscillator. It will be an amplifier with reduced gain. However, the negative feedback reduces the noise and distortion of an amplifier.

Different oscillators use different feedback networks (such as inductive coupling or LC or RC networks) for coupling the output to the input apart from the resonant circuit for obtaining oscillations of a particular frequency. These give rise to different types of oscillators like Colpitt's oscillator, Hartley oscillator, RC-oscillator, etc.

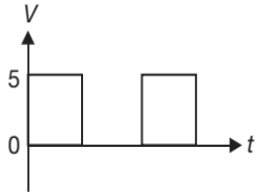
DIGITAL ELECTRONICS

Till now we have studied analog electronic circuits. In these kinds of circuits, the voltage signals vary continuously with time and such signals are called

continuous or analog voltage signals. Figure shows a typical voltage signal varying sinusoidally between 0 and 5 V.



The digital electronic circuits make use of entirely different type of voltage signals. In such signals, the pulse wave form does not vary continuously with time as in analogue voltage signals. Instead, it has only two voltage levels, either zero or some constant value of voltage. Such voltage signals are called **Digital Voltage Signals**. Figure shows a digital voltage signal, which at any instant will either be equal to 0 V or 5 V.



By representing these two voltage levels by binary numbers 0 and 1, the digital electronics has been developed. The counters, computers, etc are the outcome of digital electronics.

LOGIC GATES

A gate is a digital circuit, which works in accordance with some logical relationship between input and output voltages. Therefore, they are generally known as logic gates (gates because they control the flow of information). The five common logic gates used are OR, AND, NOT, NAND, NOR. Each logic gate is indicated by a symbol and its function is defined by a truth table that shows all the possible input logic level combinations with their respective output logic levels.

The logic gates are building blocks of digital electronics. They are used in digital electronics to change one voltage level (input voltage) into another (output voltage) according to some logical statement relating both.

A logic gate may have one input or multiple inputs, but it has only one output. The relation between the possible values of input and output voltages are expressed in the form of a table called **Truth Table or Table of Combinations**. Truth table of a logic gate is a table that shows all the input and output possibilities for the logic gate. Truth tables help us understand the behaviour of logic gates. These logic gates can be realised using semiconductor devices.

BOOLEAN ALGEBRA BASICS

1.	**Identity Law**	
	AND FORM	$1A = A$
	OR FORM	$0 + A = A$
2.	**Null Law**	
	AND FORM	$0A = 0$
	OR FORM	$1 + A = 1$
3.	**Idempotent Law**	
	AND FORM	$AA = A$
	OR FORM	$A + A = A$
4.	**Inverse Law**	
	AND FORM	$A\bar{A} = 0$
	OR FORM	$A + \bar{A} = 1$
5.	**Commutative Law**	
	AND FORM	$AB = BA$
	OR FORM	$A + B = B + A$
6.	**Associative Law**	
	AND FORM	$(AB)C = A(BC)$
	OR FORM	$A + (B + C) = (A + B) + C$
7.	**Distributive Law**	
	AND FORM	$A + BC = (A + B)(A + C)$
	OR FORM	$A(B + C) = AB + AC$
8.	**Absorption Law**	
	AND FORM	$A(A + B) = A$
	OR FORM	$A + AB = A$
9.	**De Morgan's Law**	
	AND FORM	$\overline{AB} = \bar{A} + \bar{B}$
	OR FORM	$\overline{A + B} = \bar{A}\bar{B}$

Conceptual Note(s)

Apart from the above rules please keep in mind that

(a) $\bar{1}=0$ **(b)** $\bar{0}=1$ **(c)** $1+1=1$

(d) $1+\bar{1}=1$ **(e)** $0+\bar{0}=1$

ILLUSTRATION 36

Write down truth tables for

(a) $Y=\bar{A}\bar{B}+\bar{A}B$ **(b)** $Y=(A+\bar{B})+\overline{AB}$

SOLUTION

(a)

A	B	$\bar{A}$	$\bar{B}$	$\bar{A}\bar{B}$	$\bar{A}B$	Y
0	0	1	1	1	0	1
0	1	1	0	0	1	1
1	0	0	1	0	0	0
1	1	0	0	0	0	0

(b)

A	B	$\bar{B}$	$A+\bar{B}$	AB	$\overline{AB}$	Y
0	0	1	1	0	1	1
0	1	0	0	0	1	1
1	0	1	1	0	1	1
1	1	0	1	1	0	1

ILLUSTRATION 37

Let $Y=A(\overline{BC})$. Evaluate Y for

(a) $A=1,\ B=0,\ C=1,$

(b) $A=B=C=1$ and

(c) $A=B=C=0$

SOLUTION

(a) When, $A=1,\ B=0,\ C=1$, then $BC=0$

$\Rightarrow \quad \overline{BC}=1$

$\Rightarrow \quad A\overline{BC}=1$

(b) When, $A=B=C=1$, then $BC=1$

$\Rightarrow \quad \overline{BC}=0$

$\Rightarrow \quad A\overline{BC}=0$

(c) When, $A=B=C=0$, then $BC=0$

$\Rightarrow \quad \overline{BC}=1$

$\Rightarrow \quad A\overline{BC}=0$

ILLUSTRATION 38

Let $Y=A\overline{BC}+B\overline{CA}+C\overline{AB}$. Find the output Y if following inputs are given

(a) $A=1,\ B=0,\ C=1$

(b) $A=B=C=1$

(c) $A=B=C=0$

SOLUTION

A	B	C	$\overline{AB}$	$\overline{BC}$	$\overline{CA}$	$A\overline{BC}$	$B\overline{CA}$	$C\overline{AB}$	Y
0	0	0	1	1	1	0	0	0	0
1	1	1	0	0	0	0	0	0	0
1	0	1	1	1	0	1	0	1	1

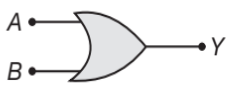
(a) $Y=1$ **(b)** $Y=0$ **(c)** $Y=0$

THE 'OR GATE'

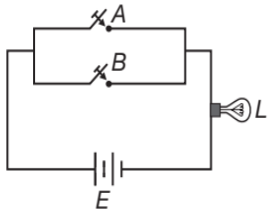
The OR gate is a two inputs and one output logic gate. It combines the inputs A and B with the output Y following the Boolean expression

$$Y=A+B$$

to be read as Y equals A OR B. The symbol of OR gate, its electrical analogue and its truth table are shown.



SYMBOL

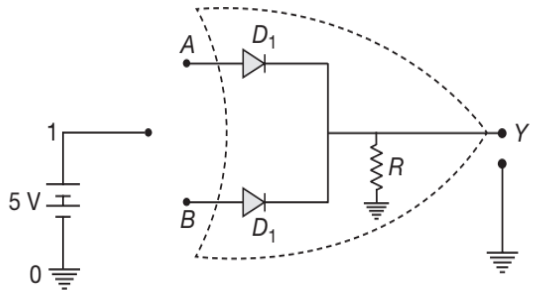


ELECTRICAL ANALOGUE

A	B	Y
0	0	0
1	0	1
0	1	1
1	1	1

Realisation of OR Gate

The negative terminal of the battery is grounded and corresponds to the 0 state and the positive (i.e., voltage 5 V in the present case) to the 1 state.



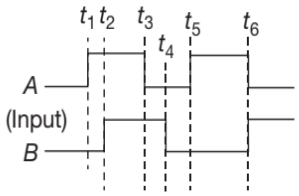
When both A and B are connected to 0, no current passes through the diode and therefore no voltage develops across R and the output is zero.

When input A is connected to zero and B to 1, the diode D_2 is forward biased and the current through it is limited by a current limiting resistance. This current causes a 5 V drop across the resistance assuming the diode to be ideal and this gives an output of 5 V or 1. Interchanging A and B to 1 and 0 will still give a 5 V drop across the resistance as D_1 will conduct.

When the terminals A and B are connected to 1, then both the diodes D_1 and D_2 conduct. However, the voltage drop across R cannot exceed 5 V and the output is 1. Hence the truth table is satisfied.

ILLUSTRATION 39

For the input waveforms A and B shown in Figure, sketch the output waveform (Y) obtained from OR gate.



SOLUTION

Note the following:

(a) At $t < t_1$; $A = 0$, $B = 0$; Hence $Y = 0$

(b) For t_1 to t_2; $A = 1$, $B = 0$; Hence $Y = 1$

(c) For t_2 to t_3; $A = 1$, $B = 1$; Hence $Y = 1$

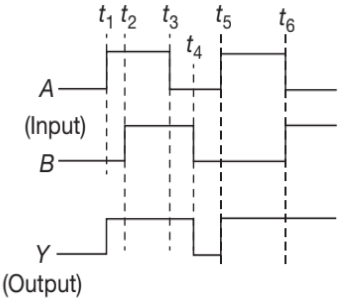
(d) For t_3 to t_4; $A = 0$, $B = 1$; Hence $Y = 1$

(e) For t_4 to t_5; $A = 0$, $B = 0$; Hence $Y = 0$

(f) For t_5 to t_6; $A = 1$, $B = 0$; Hence $Y = 1$

(g) For $t > t_6$; $A = 0$, $B = 1$; Hence $Y = 1$

Therefore, the waveform Y will be as shown in the figure.

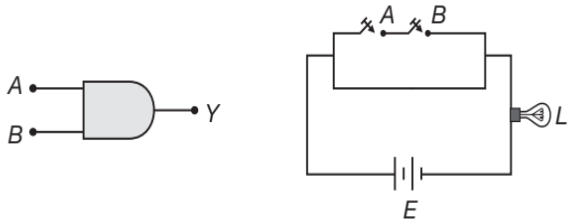


THE AND GATE

The AND gate is also a two inputs and one output logic gate. It combines the inputs A and B with the output Y following the Boolean expression

$$Y = A \cdot B$$

to be read as Y equals A AND B. The symbol of AND gate its electrical analogue and its truth table are shown.

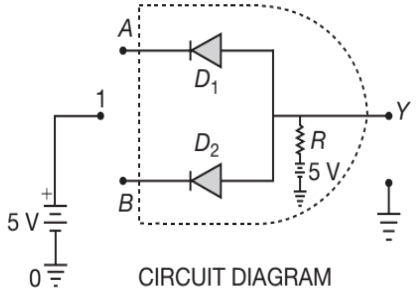


A	B	Y
0	0	0
1	0	0
0	1	0
1	1	1

Realisation of AND Gate

The resistor R is connected permanently to the positive terminal of a 5 V battery. When both A and B are connected to zero, both the diodes conduct.

The voltage output at Y will be the voltage across the diode which is 0 assuming the diodes to be ideal.



CIRCUIT DIAGRAM

When A is connected to 0 and B to 1, the upper diode conducts while lower diode does not conduct as it is not forward biased. The voltage output of Y will then be the voltage across the upper diode which is 0.

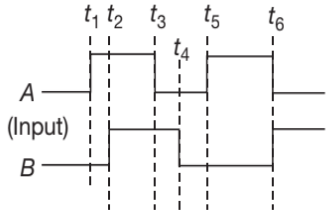
When A is 1 and B is 0, the lower diode conducts and the output is 0.

When both A and B are connected to 1, none of the diodes conduct. Hence the voltage at the output Y will be the battery voltage i.e., Y will be 1.

Thus, we see that the circuit in figure can perform the function of an AND gate. We note that the output is 1 only when both the inputs are 1.

ILLUSTRATION 40

For the input waveforms A and B shown in Figure, sketch the output waveform (Y) obtained from AND gate.



SOLUTION

(a) For $t \le t_1$; $A = 0$, $B = 0$; Hence $Y = 0$

(b) For t_1 to t_2; $A = 1$, $B = 0$; Hence $Y = 0$

(c) For t_2 to t_3; $A = 1$, $B = 1$; Hence $Y = 1$

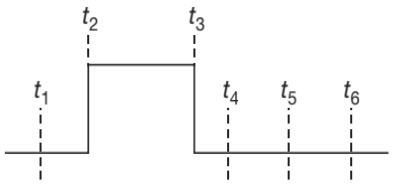
(d) For t_3 to t_4; $A = 0$, $B = 1$; Hence $Y = 0$

(e) For t_4 to t_5; $A = 0$, $B = 0$; Hence $Y = 0$

(f) For t_5 to t_6; $A = 1$, $B = 0$; Hence $Y = 0$

(g) For $t > t_6$; $A = 0$, $B = 1$; Hence $Y = 0$

Based on the above, the output waveform for AND gate can be drawn as given below.

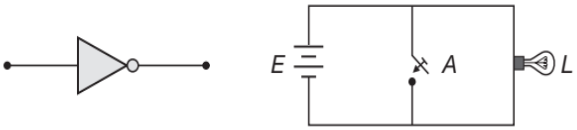


THE 'NOT GATE'

The NOT gate is a one input and one output logic gate. It combines the input A with the output Y following the Boolean expression

$$Y = \overline{A}$$

to be read as Y equals NOT A. The way, the NOT gate gives the output, it is also called **Invertor or Negator**. It is represented by the symbol as shown in figure.

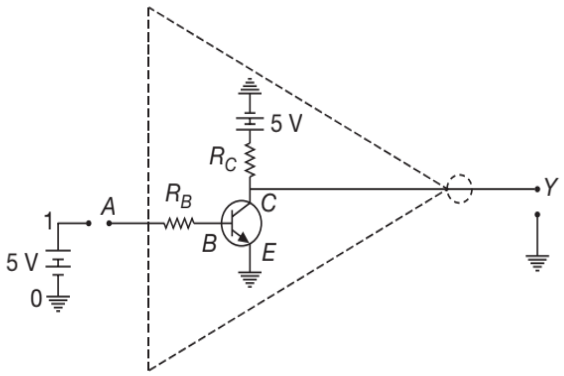


SYMBOL ELECTRICAL ANALOGUE

A	Y
0	1
1	0

Realisation of NOT Gate

A NOT gate cannot be realised by diodes and we have to use a transistor. We choose R_B and R_C such that when 5 V (or voltage corresponding to 1 state) is applied at the base, a large collector current flows, the voltage at Y drops and the base-collector junction is forward-biased.



When A is connected to 0, the collector base is reverse biased and the base emitter junction is not forward biased. So the base current is zero and hence the collector current is zero. The transistor is then said to be in the cut-off mode and the voltage at Y is 5 V, which corresponds to the 1 state. When A is connected to 1, the transistor goes to saturation, the voltage drop across R_C is almost equal to 5 V and the output Y is very nearly 0 V corresponding to 0 of truth table.

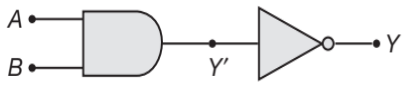
COMBINATION OF GATES

Various combinations of three basic gates i.e. OR, AND and NOT give rise to complicated digital circuits. We now discuss a few combinations of these basic gates using their symbols,

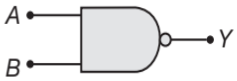
The NAND Gate

It is a logic circuit in which AND gate is followed by a NOT gate.

If the output (Y') of AND gate is connected to the input of NOT gate, the gate so obtained is called NAND gate. The logic symbol of the NAND gate is as shown in figure.



(a)



(b)

The truth table of NAND gate can be obtained by combining the truth tables of AND and NOT gates. It will be as given in figure.

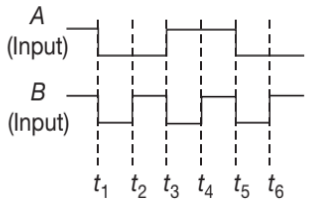
A	B	Y	Y'
0	0	0	1
1	0	0	1
0	1	0	1
1	1	1	0

Boolean expression for the NAND gate is

$$Y = \overline{AB}$$

ILLUSTRATION 41

Sketch the output Y from a NAND gate having inputs A and B shown in Figure.



SOLUTION

(a) For $t < t_1$; $A = 1$, $B = 1$; Hence $Y = 0$

(b) For t_1 to t_2; $A = 0$, $B = 0$; Hence $Y = 1$

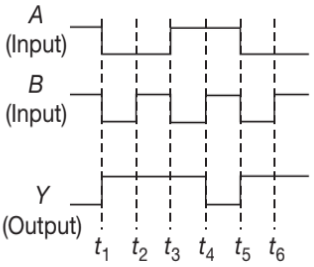
(c) For t_2 to t_3; $A = 0$, $B = 1$; Hence $Y = 1$

(d) For t_3 to t_4; $A = 1$, $B = 0$; Hence $Y = 1$

(e) For t_4 to t_5; $A = 1$, $B = 1$; Hence $Y = 0$

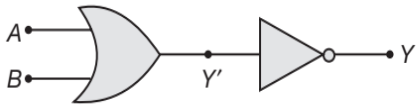
(f) For t_5 to t_6; $A = 0$, $B = 0$; Hence $Y = 1$

(g) For $t > t_6$; $A = 0$, $B = 1$; Hence $Y = 1$

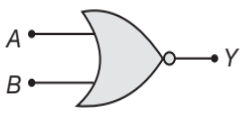


The NOR Gate

It is a logic circuit in which OR gate is followed by a NOT gate. If the output (Y') of OR gate is connected to the input of a NOT gate, the gate so obtained is called the NOR gate. The logic symbol of the NOR gate is shown in figure.



(a)



(b)

The truth table of NOR gate can be obtained by combining the truth tables of OR and NOT gates.

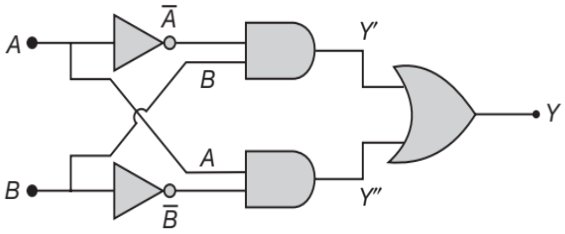
A	B	Y′	Y
0	0	0	1
1	0	1	0
0	1	1	0
1	1	1	0

Boolean expression for the NOR gate is

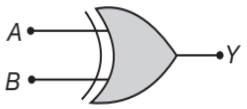
$$Y = \overline{A+B}$$

THE 'XOR GATE'

XOR gate is obtained by using OR, AND and NOT gates as shown in figure. It is also called **Exclusive OR gate** and its logic symbol is as shown in figure.



(a)



(b)

Its truth table is given in figure. It follows that output in case of XOR gate is 1, only when inputs are different.

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

The Boolean equation for the XOR gate is

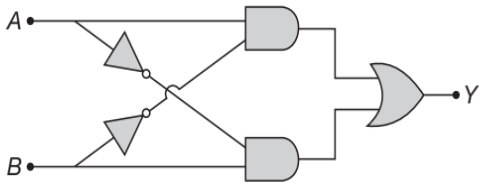
$$Y = A\bar{B} + \bar{A}B$$

Conceptual Note(s)

The NAND and the NOR gates are the building blocks of the digital electronics, because all the logic gates like the OR, the AND, the NOT can be constructed by using the NAND gates or by using the NOR gates.

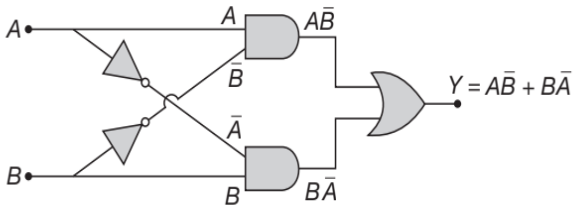
ILLUSTRATION 42

Write the truth table for the circuit given in figure.



SOLUTION

The circuit can be redrawn as,



The corresponding truth table is

A	B	$\bar{A}$	$\bar{B}$	$A\bar{B}$	$B\bar{A}$	Y
0	0	1	1	0	0	0
0	1	1	0	0	1	1
1	0	0	1	1	0	1
1	1	0	0	0	0	0

LOGIC GATES USING NAND GATES

Construction of the 'NOT' gate from the 'NAND' gate

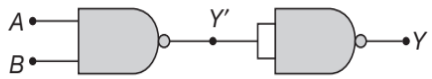
When both the inputs (A and B) of the NAND gate are joined together then it works as the NOT gate.

Truth table and logic symbol

Input	Output
$A = B$	Y
0	1
1	0

Construction of the 'AND' gate from the 'NAND' gate

When the output of the NAND gate is given to the input of the NOT gate (made from the NAND gate), then the resultant logic gate works as the AND gate

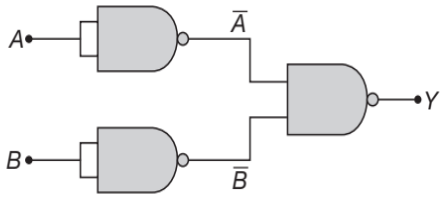


Truth table and logic symbol

A	B	Y'	Y
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	1

Construction of the 'OR' gate from the 'NAND' gate

When the outputs of two NOT gates (obtained from the NAND gate) is given to the inputs of the NAND gate, the resultant logic gate works as the OR gate



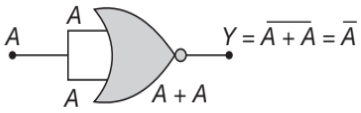
Truth table and logic symbol

A	B	$\overline{A}$	$\overline{B}$	Y
0	0	1	1	0
0	1	1	0	1
1	0	0	1	1
1	1	0	0	1

LOGIC GATES USING NOR GATES

Construction of the 'NOT' gate from the 'NOR' gate

When both the inputs (A and B) of the NAND gate are joined together then it works as the NOT gate.



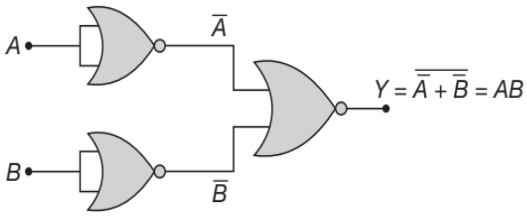
NOT Gate

Truth table and logic symbol

Input	Output
0	1
1	0

Construction of the 'AND' gate from the 'NOR' gate

When the output of the NAND gate is given to the input of the NOT gate (made from the NAND gate), then the resultant logic gate works as the AND gate



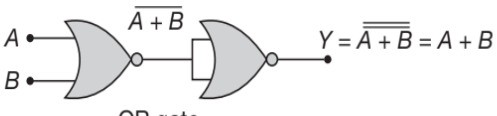
AND gate

Truth table and logic symbol

A	B	Y = AB
0	0	0
0	1	0
1	0	0
1	1	1

Construction of the 'OR' gate from the 'NOR' gate

When the outputs of two NOT gates (obtained from the NAND gate) is given to the inputs of the NAND gate, the resultant logic gate works as the OR gate



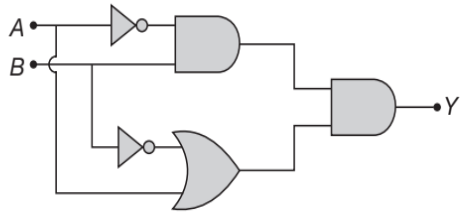
OR gate

Truth table and logic symbol

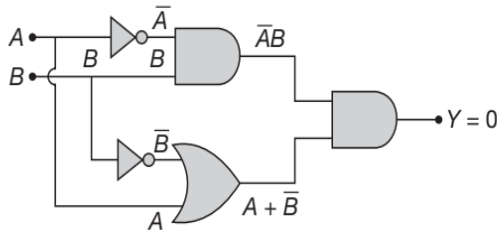
A	B	Y = A + B
0	0	0
0	1	1
1	0	1
1	1	1

ILLUSTRATION 43

Find the output Y and write the truth table for the following circuit.



SOLUTION



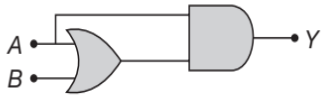
$Y = \bar{A}B(A+\bar{B})$

$Y = A\bar{A}B + \bar{A}\bar{B}B = 0$

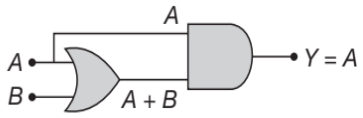
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	0

ILLUSTRATION 44

Find the output Y and write the truth table for the following circuit.



SOLUTION



$Y = A(A+B)$

$\Rightarrow \quad Y = A + AB$

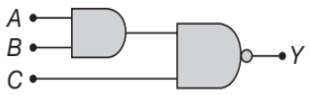
$\Rightarrow \quad Y = A(1+B)$

$\Rightarrow \quad Y = A$

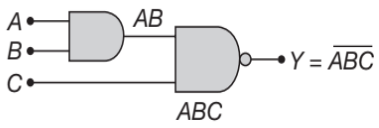
A	B	Y
0	0	0
0	1	0
1	0	1
1	1	1

ILLUSTRATION 45

Find the output Y when all inputs are first high and then low.



SOLUTION



Since, $Y = \overline{ABC}$

When all inputs are high i.e. $A = 1$, $B = 1$, $C = 1$ then

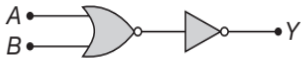
$Y = \bar{1} = 0$

When all inputs are low i.e. $A = 0$, $B = 0$, $C = 0$ then

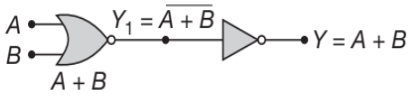
$Y = \bar{0} = 1$

ILLUSTRATION 46

Write the truth table for the following circuit. Name the equivalent gate that this circuit represents.



SOLUTION

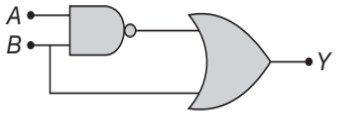


A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

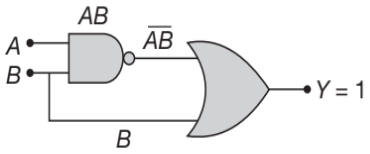
From the truth table, it is clear that the output is high only when atleast one of the inputs is high (i.e. 1). So, the circuit corresponds to OR gate.

ILLUSTRATION 47

Write the Boolean equation for the following circuit. Also write the truth table.



SOLUTION



$$Y = \overline{AB} + B$$

According to de-Morgan's Law

$$\overline{AB} = \overline{A} + \overline{B}$$

$$\Rightarrow \quad Y = \overline{AB} + B = \overline{A} + \overline{B} + B$$

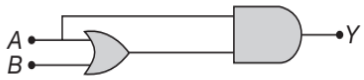
Since, $B + \overline{B} = 1$

$$\Rightarrow \quad Y = \overline{A} + 1 = 1$$

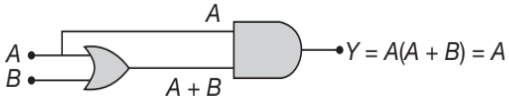
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	1

ILLUSTRATION 48

Draw the truth table for the function Y of A and B for the following logic gate.



SOLUTION



The output Y in terms of the input A and B can be written as,

$$Y = A(A + B)$$

$$\Rightarrow \quad Y = AA + AB$$

Since, $AA = A$

$$\Rightarrow \quad Y = A + AB = A(1 + B)$$

Since, $1 + B = 1$

$$\Rightarrow \quad Y = A$$

The truth table for the logic gate is

A	B	Y = A
0	0	0
0	1	0
1	0	1
1	1	1

SOLVED PROBLEMS

PROBLEM 1

In a silicon sample, the number density of silicon atoms is $5\times10^{28}\ \text{m}^{-3}$. This sample is doped simultaneously with $5\times10^{22}\ \text{m}^{-3}$ atoms of arsenic and $5\times10^{20}\ \text{m}^{-3}$ atoms of indium. Calculate the number density of electrons and holes. Given that $n_i = 1.5\times10^{16}\ \text{m}^{-3}$. Is the sample p-type or n-type.

SOLUTION

Since we know that, for each atom doped of arsenic one free electron is received and for each atom doped of indium a vacancy is created. So, the number of free electrons introduced by adding the pentavalent impurity is

$$n_e = N_{As} = 5\times10^{22}\ \text{m}^3 \qquad \ldots(1)$$

The number of holes introduced by adding the trivalent impurity is

$$n_e - n_h = 5\times10^{22} - 5\times10^{20}$$

$$\Rightarrow \quad n_e - n_h = 4.95\times10^{22} \qquad \ldots(2)$$

Since we know that

$$(n_e + n_h)^2 = (n_e - n_h)^2 + 4n_e n_h$$

Also, $n_e n_h = n_i^2$

$$\Rightarrow \quad (n_e + n_h)^2 = (n_e - n_h)^2 + 4n_i^2$$

$$\Rightarrow \quad n_e + n_h = \sqrt{(4.95\times10^{22})^2 + 4(1.5\times10^{16})^2}$$

$$\Rightarrow \quad n_e + n_h = 4.95\times10^{22} \qquad \ldots(3)$$

Adding Equations (3) and (2), we get

$$2n_e = 2(4.95\times10^{22})$$

$$\Rightarrow \quad n_e = 4.95\times10^{22}\ \text{m}^{-3}$$

Since $n_i^2 = n_h n_e$

$$\Rightarrow \quad n_h = \frac{n_i^2}{n_e} = \frac{(1.5\times10^{16})^2}{4.95\times10^{22}} = 4.54\times10^{9}\ \text{m}^{-3}$$

Now, since the number density of electrons $n_e\,(=4.95\times10^{22})$ is greater than number of holes $n_h\,(=4.5\times10^{9})$. So, the sample is an n-type semiconductor.

PROBLEM 2

Suppose the number density of silicon atoms in a pure silicon is $5\times10^{28}\ \text{m}^{-3}$. It is doped by 1 ppm concentration of arsenic atoms. Calculate the number of electrons and holes. Given that $n_i = 1.5\times10^{16}\ \text{m}^{-3}$.

SOLUTION

Since, $n_i = 1.5\times10^{16}\ \text{m}^{-3}$

Doping concentration of pentavalent arsenic atoms is 1 ppm i.e. 1 part per million
So, number density of pentavalent arsenic atoms is

$$N_d = \frac{5\times10^{28}}{10^6} = 5\times10^{22}\ \text{atom m}^{-3}$$

Since the thermally generated electrons $(n_i \propto 10^{16}\ \text{m}^{-3})$ are negligibly small as compared to those produced by doping, so

$$n_e \approx N_d = 5\times10^{22}\ \text{m}^{-3}$$

Also, $n_e n_h = n_i^2$

$$\Rightarrow \quad n_h = \frac{n_i^2}{n_e} = \frac{1.5\times10^{16}\times1.5\times10^{16}}{5\times10^{22}}$$

$$\Rightarrow \quad n_h = 4.5\times10^{9}\ \text{m}^{-3}$$

PROBLEM 3

A pure germanium plate of area $3.5\times10^{-4}\ \text{m}^2$ and of thickness 1.5×10^{-3} m is connected across a battery of potential 5 V. Calculate the amount of current produced at room temperature in the germanium sample. Also find the amount of heat generated in the plate in 120 second. Given that the concentration of carriers in germanium at room temperature is 1.6×10^{6} per cubic metre. The mobilities of electrons and holes are $0.4\ \text{m}^2\text{V}^{-1}\text{s}^{-1}$ and $0.2\ \text{m}^2\text{V}^{-1}\text{s}^{-1}$ respectively.

SOLUTION

Conductivity of semiconductor is given by

$$\sigma = n_e e\mu_e + n_h e\mu_h$$

Since semiconductor is intrinsic, so we have

$$n_e = n_h = n_i$$

$$\Rightarrow \quad \sigma = n_i e(\mu_e + \mu_h)$$

$$\Rightarrow \quad \sigma = 1.6\times10^{6}\times1.6\times10^{-19}(0.4+0.2)$$

$$\Rightarrow \quad \sigma = 1.536\times10^{-13}\ \text{ohm}^{-1}\text{m}^{-1}$$

Current flowing is given by

$$i = jA$$

where, j is the current density given by

$$j = \sigma E = \sigma\left(\frac{V}{d}\right)$$

$$\Rightarrow \quad i = \sigma\left(\frac{V}{d}\right)A$$

$$\Rightarrow \quad i = (1.536\times10^{-13})\left(\frac{5}{1.5\times10^{-3}}\right)(3.5\times10^{-4})$$

$$\Rightarrow \quad i = 1.79\times10^{-13}\ \text{A}$$

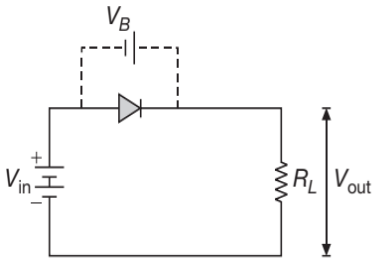
Heat produced is given by

$$H = Vit = 5\times1.79\times10^{-13}\times120$$

$$\Rightarrow \quad H = 10.74\times10^{-11}\ \text{J}$$

PROBLEM 4

A silicon diode is connected to a battery having voltage $V_{in} = 10$ V and a load resistance $R_L = 10$ kΩ as shown in Figure.



If the barrier voltage is $V_B = 0.7$ V, then calculate the output voltage across R_L, current in the diode and the forward resistance.
Assuming the diode to be ideal, calculate the output voltage and output current in diode.

SOLUTION

Since, $V_{out} = V_{in} - V_B$, where V_B is the barrier voltage

$$\Rightarrow \quad V_{out} = 10 - 0.7 = 9.3\ \text{V}$$

As diode is in forward biased state, so it will conduct

$$\Rightarrow \quad I = \frac{V_{out}}{R_L} = \frac{9.3}{10\times10^{3}} = 0.9\ \text{mA}$$

and, $r_f = \dfrac{V_B}{I} = \dfrac{0.7}{0.9\times10^{-3}} = 777\ \Omega$

For ideal diode, $r_f = 0$, $V_B = 0$

$$V_{out} = V_{in} = 10\ \text{V}$$

$$I = \frac{V_{out}}{R_L} = \frac{10}{10\times10^{3}} = 1\ \text{mA}$$

PROBLEM 5

A semiconductor diode is used as a half rectifier having internal resistance $200\ \Omega$. The voltage applied is given by $V = 50\sin(\omega t)$ volt and load resistance is $650\ \Omega$. Calculate the maximum output current, dc output current, dc output power and dc output voltage.

SOLUTION

Given that $V = 50\sin(\omega t)$ volt

Comparing it with general equation $V = V_0\sin(\omega t)$, we get

$$V_0 = 50\ \text{volt}$$

Also, it is given that $R_L = 650\ \Omega$, $r_d = 200\ \Omega$

Maximum output current is

$$I_0 = \frac{V_0}{r_d + R_L}$$

$$\Rightarrow \quad I_0 = \frac{50}{(200+650)} = 58\ \text{mA}$$

dc output current is

$$I_{DC} = \frac{I_0}{\pi} = 18.5\ \text{mA}$$

dc output power is

$$P = I_{dc}^2 R_L = 0.22\ \text{W}$$

dc output voltage is

$$V = I_{dc}R_L = 12.02\ \text{W}$$

PROBLEM 6

In an npn transistor used in common emitter mode, 10^{10} electrons enter the emitter in 10^{-6} s. If only 2% of the electrons are lost in the base. Calculate the base

current and the current amplification factor. Given that the charge on an electron is 1.6×10^{-19} C.

SOLUTION

The current in the emitter is given by

$$I_E=\frac{q}{t}=\frac{10^{10}\times1.6\times10^{-19}}{10^{-6}}=1.6\text{ mA}$$

Since, base current I_B is 2% of I_E, so we have

$$I_B=\left(\frac{2}{100}\right)\times1.6\text{ mA}=0.032\text{ mA}$$

$$\Rightarrow\quad I_C=I_E-I_B=1.568\text{ mA}$$

So, the current amplifications factor is given by

$$\beta=\frac{I_C}{I_B}=\frac{1.568}{0.032}=49$$

PROBLEM 7

In a common emitter amplifier, the load resistance of the output circuit is 500 times the resistance of the input circuit. If $\alpha=0.98$, then find the voltage gain and power gain.

SOLUTION

Given that, $\alpha=0.98$ and $\frac{R_{\text{out}}}{R_{\text{in}}}=5000$,

Since, $\beta=\frac{\alpha}{1-\alpha}=\frac{0.98}{1-0.98}=49$

$$\Rightarrow\quad \beta=\frac{0.98}{1-0.98}=49$$

Voltage gain is

$$A_V=(\beta)\left(\frac{R_{\text{out}}}{R_{\text{in}}}\right)=(49)(500)=24500$$

Power gain is

$$A_P=(\beta^2)\left(\frac{R_{\text{out}}}{R_{\text{in}}}\right)=(49)^2(500)=1200500$$

PROBLEM 8

A transistor is used in common emitter mode in an amplifier circuit. When a signal of 40 mV is added to the base-emitter voltage, the base current changes by 40 μA and the collector current changes by 4 mA. The load resistance is 5 kΩ. Calculate the current gain β, the input resistance R_i, the transconductance g_m and the voltage gain.

SOLUTION

Given that $\Delta I_B=40\ \mu\text{A}$ and $\Delta I_C=4\text{ mA}$

$$\beta=\frac{\Delta I_C}{\Delta I_B}=\frac{4\times10^{-3}}{40\times10^{-6}}=100$$

Since, $\Delta V_i=(\Delta I_B)\times R_i$

$$\Rightarrow\quad R_i=\frac{\Delta V_i}{\Delta I_B}=\frac{40\times10^{-3}}{40\times10^{-6}}=1000\ \Omega=1\text{ k}\Omega$$

The transconductance g_m is

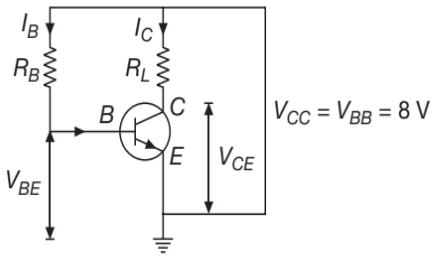
$$g_m=\frac{\Delta I_C}{\Delta V_i}=\frac{4\times10^{-3}}{40\times10^{-3}}=0.1\ \Omega^{-1}$$

The voltage gain A_V is

$$A_V=\beta\left(\frac{R_{\text{out}}}{R_{\text{in}}}\right)=(100)\left(\frac{5}{1}\right)=500$$

PROBLEM 9

An n-p-n transistor in a common emitter mode is used as a simple voltage amplifier with a collector current of 4 mA. The terminal of 8 V battery is connected to the collector through a load resistance R_L and to the base through a resistance R_B. The collector emitter voltage $V_{CE}=4$ V, base emitter voltage $V_{BE}=0.6$ V and base current amplification factor $\beta_{DC}=100$. Calculate the values of R_L and R_B.



SOLUTION

Given that, $V_{CE}=4$ V, $V_{BE}=0.6$ V, $\beta=100$

and $\Delta I_C=4\text{ mA}=4\times10^{-3}$ A

Since, $V_{CE}=V_{CC}-I_CR_L$

$$\Rightarrow\quad V_{CE}+\Delta I_CR_L=V_{CC}$$

$$\Rightarrow\quad 4\times10^{-3}R_L=8-4=4$$

$$\Rightarrow\quad R_L=1000\ \Omega$$

The base current is given by

$$I_B = \frac{I_C}{\beta} = \frac{4\times10^{-3}}{100} = 4\times10^{-5}\ \text{A}$$

Also, we know that

$$V_{CC} = I_B R_B + V_{BE}$$

$$\Rightarrow \quad 8 = I_B R_B + 0.6$$

$$\Rightarrow \quad I_B R_B = 7.4\ \text{V}$$

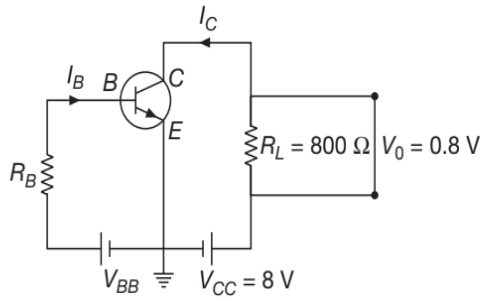
$$\Rightarrow \quad 4\times10^{-5} R_B = 7.4$$

$$\Rightarrow \quad R_B = \frac{7.4}{4}\times10^5 = 1.85\times10^5\ \Omega$$

$$\Rightarrow \quad R_B = 185\ \text{k}\Omega$$

PROBLEM 10

An npn transistor is connected in common emitter configuration in which collector supply is 8 V and the voltage drop across the load resistance of 800 Ω connected in the collector circuit is 0.8 V . If current gain factor is $\left(\frac{25}{26}\right)$, determine the collector emitter voltage and base current. If the internal resistance of the transistor is 200 Ω , calculate the voltage gain and power gain.



SOLUTION

Since, $V_0 = I_C R_L$

$$\Rightarrow \quad 0.8 = I_C \times 800$$

$$\Rightarrow \quad I_C = 10^{-3}\ \text{A}$$

Since, $V_{CE} = V_{CC} - I_C R_L$

$$\Rightarrow \quad V_{CC} = V_{CE} + I_C R_L$$

$$\Rightarrow \quad 8 = V_{CE} + 10^{-3}\times800$$

$$\Rightarrow \quad V_{CE} = 8 - 0.8 = 7.2\ \text{V}$$

Since the current gain factor is given to be $\frac{25}{26}$, which is less than 1, so it must be the current gain for the common base configuration of the transistor.

$$\Rightarrow \quad \alpha = \frac{25}{26},$$

$$\Rightarrow \quad \beta = \frac{\alpha}{1-\alpha} = \frac{\frac{25}{26}}{1-\frac{25}{26}} = 25$$

$$\Rightarrow \quad I_B = \frac{I_C}{\beta} = \frac{10^{-3}}{25} = 4\times10^{-5}\ \text{A} = 40\ \mu\text{A}$$

Voltage gain is

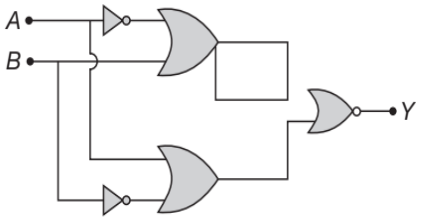
$$A_V = \beta\frac{R_L}{r_i} = 25\times\frac{800}{200} = 100$$

Power gain is

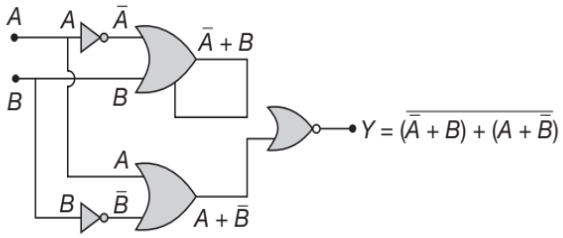
$$A_p = \beta^2\frac{R_L}{r_i} = \beta A_V = 25(100) = 2500$$

PROBLEM 11

Construct truth table for the function Y of A and B as shown in the figure.



SOLUTION



The Boolean expression of the output is

$$Y = (\bar{A}+B)+(A+\bar{B})$$

$$\Rightarrow \quad Y = (\bar{A}+A)+(B+\bar{B})$$

Since, $A+\bar{A}=0$ and $B+\bar{B}=0$

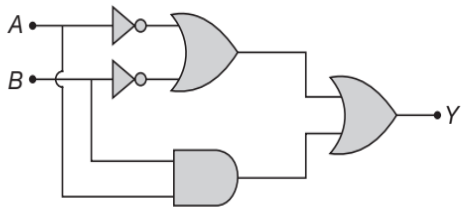
$$\Rightarrow \quad Y = 0$$

The corresponding truth table is

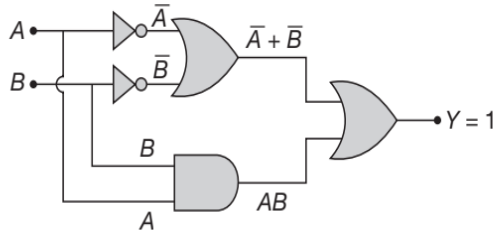
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	0

PROBLEM 12

Write the Boolean equation and truth table for the following circuit. Also draw the output wave form.



SOLUTION



$$Y = AB + \bar{A} + \bar{B}$$

According to de-Morgan's Law

$$\bar{A} + \bar{B} = \overline{AB}$$

$$\Rightarrow \quad Y = AB + \overline{AB}$$

$$\Rightarrow \quad Y = 1$$

The truth table for the above combination of logic gates is

A	B	AB	$\overline{AB}$	Y
0	0	0	1	1
1	0	0	1	1
0	1	0	1	1
1	1	1	0	1

The output wave form for the circuit is shown in Figure.